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39	+3V_S5/+5V_S5(RT6575AGQW)
40	+VDDQ (RT8231B)
41	+1V_S5 (TPS51211)
42	+1.8V_S5 (RT8068A)
43	CPU VR (NCP81206)
44	+VCCORE / +VCCGT
45	+VCCSA (NCP81253)
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Intel Skylake-U Platform

Skylake-U CPU (TDP 15W) SoC

Project Information


Phase: EVT

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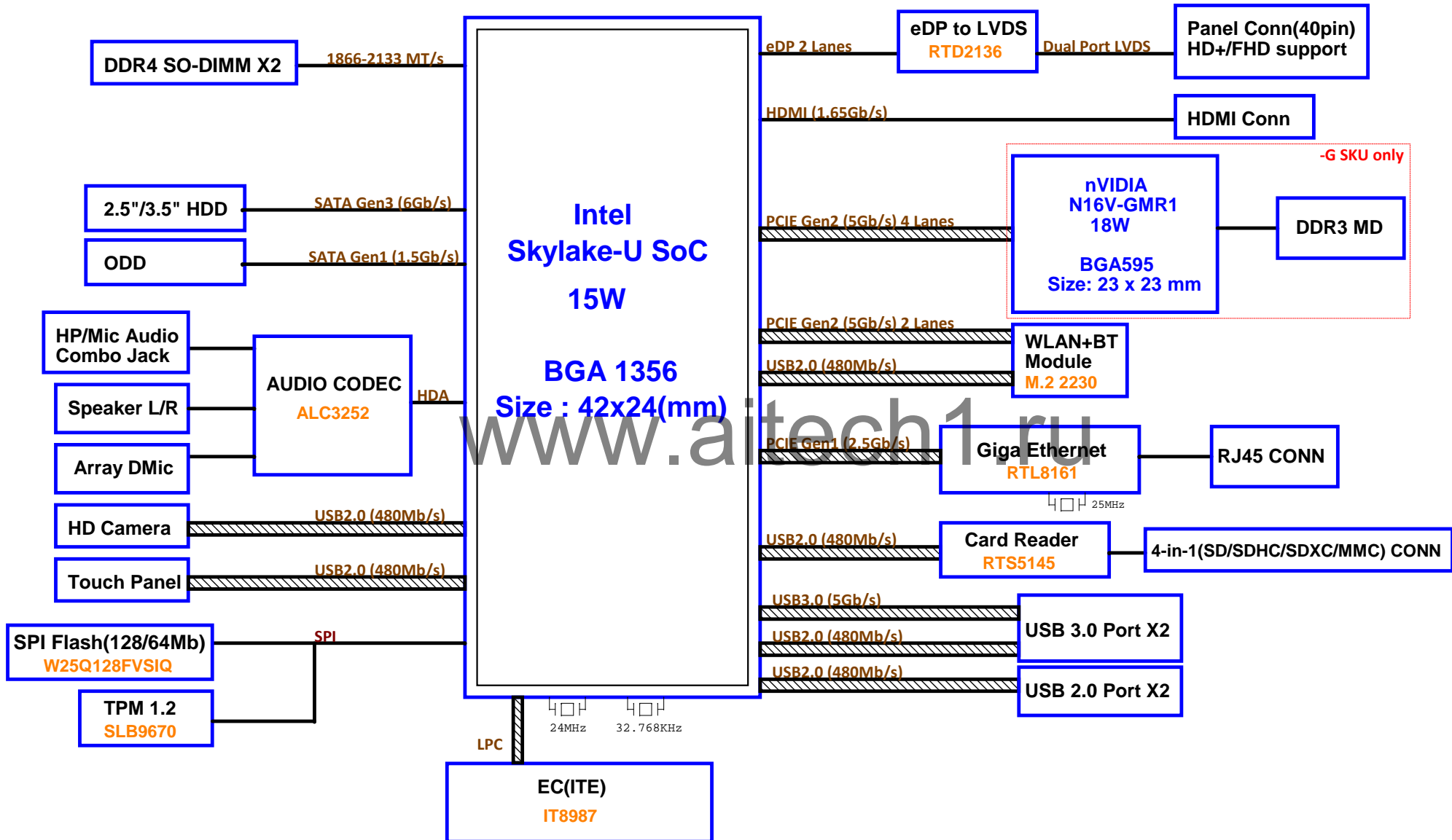
PCB AND SILKSCREEN COLOR

Program Phase	Color of PCB	Silkscreen
EVT	RED	YELLOW
DVT	LIGHT BLUE	YELLOW
PVT/MVB / PRODUCTION	GREEN	WHITE

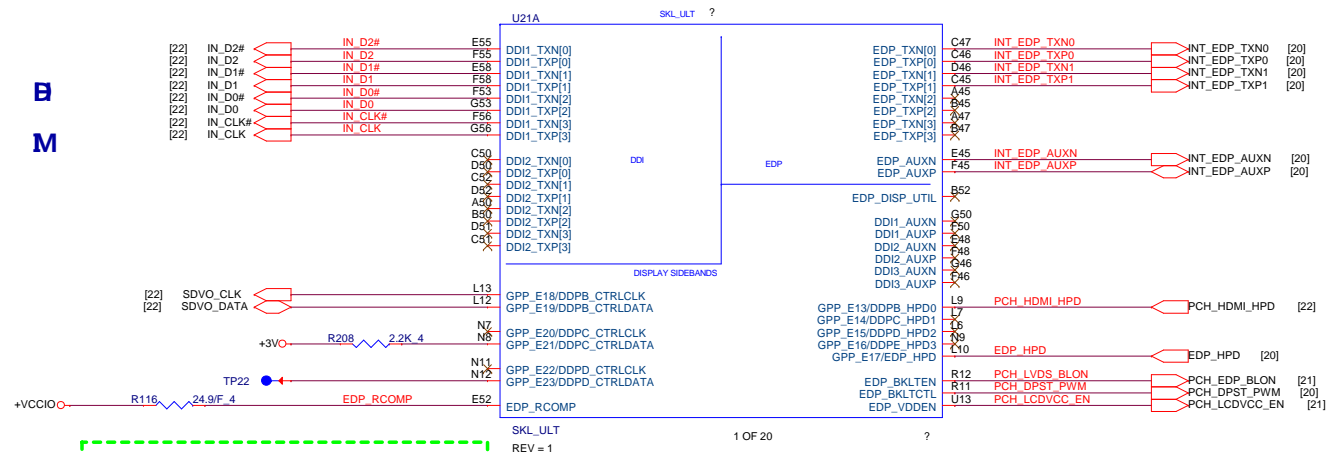
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		PROJECT: HP-Hawaii	
Size Custom	Document Number Front Page	Rev 1A	
Date: Thursday, December 17, 2015	Sheet	1	of 58

Intel Skylake-U Platform Block Diagram (Hawaii-G/-U)

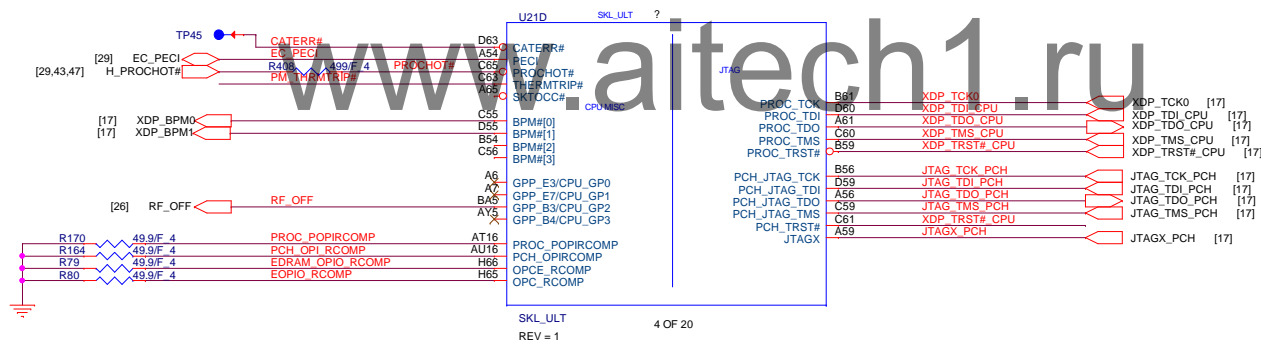
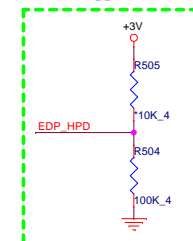


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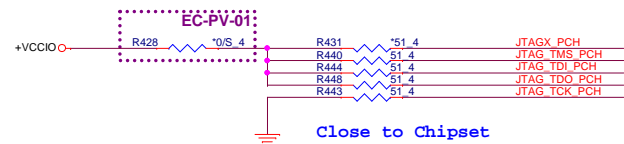
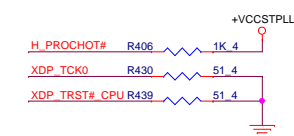
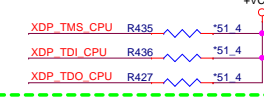
eDP_COMPIO and ICOMPIO signals should be shorted near balls and routed with typical impedance <25 mohms

Reserve EDP_HPD opposites circuit!



Processor pull-up (CPU)
TO BE REPLACED WITH 1K OHMS FOR SKL .
470 OHM IS FOR I/P

PLACE NEAR CPU



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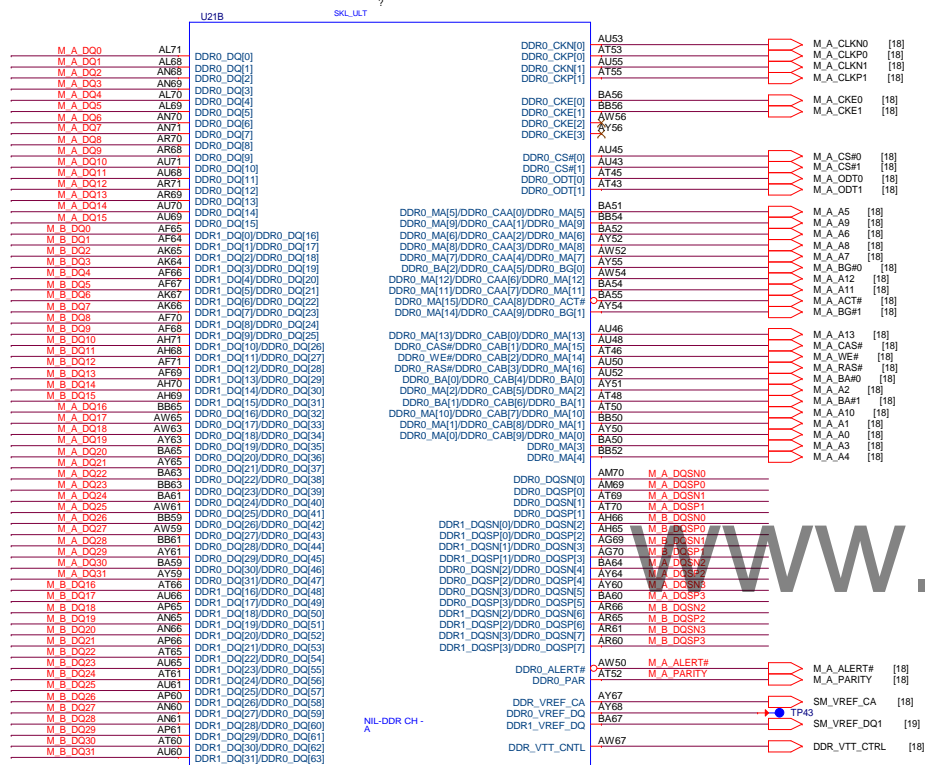
Quanta Computer Inc.

PROJECT: HP-Hawaii

Size Custom Document Number SKL CPU eDP/DDI/MISC Rev 1A

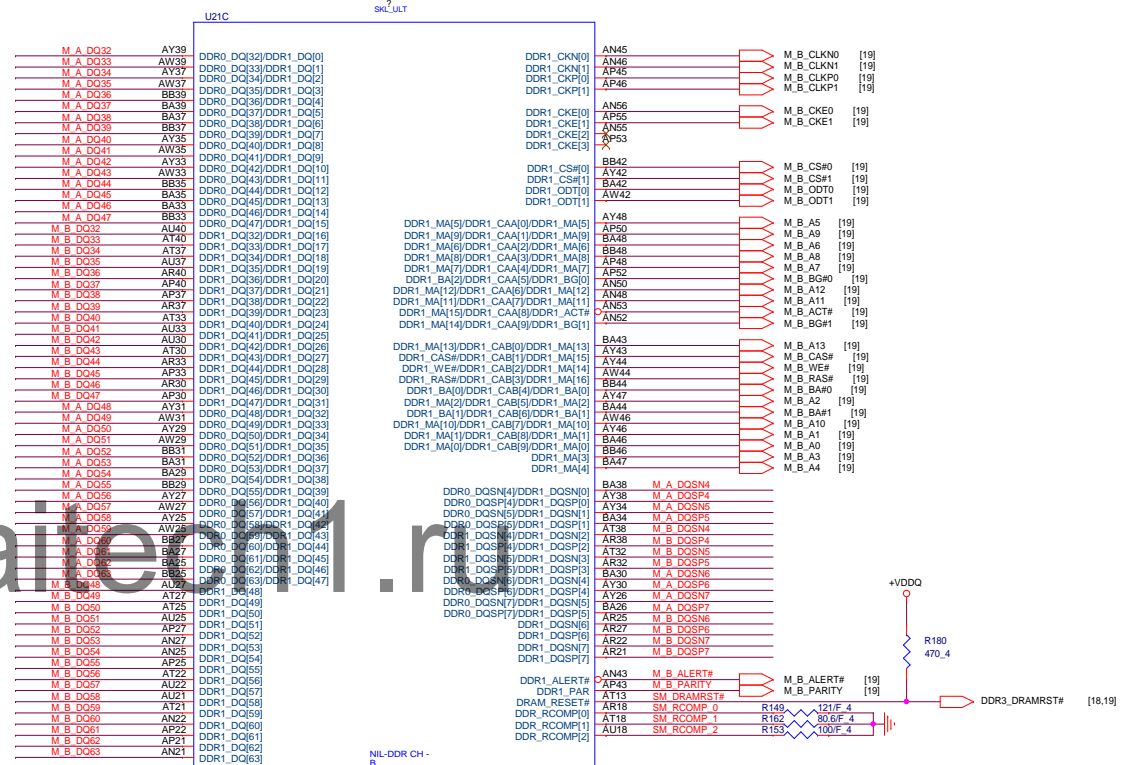
Date: Wednesday, March 09, 2016 Sheet 3 of 58

SkyLake ULT Processor (DDR4 IL)



SKL_ULT
REV = 1

2 OF 20



SKL_ULT
REV = 1

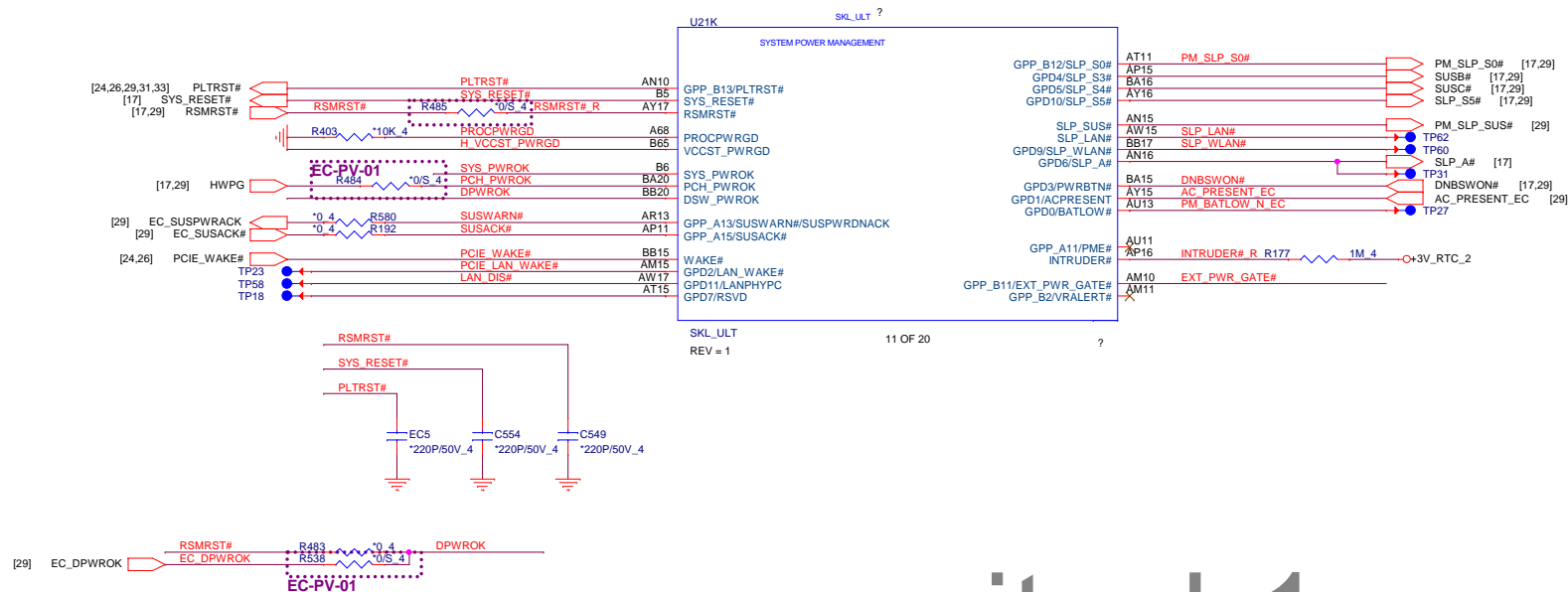
3 OF 20

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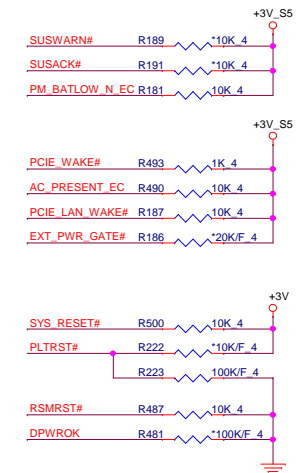


Size Custom	Document Number SKL CPU DDR	Rev 1A
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8V
1A

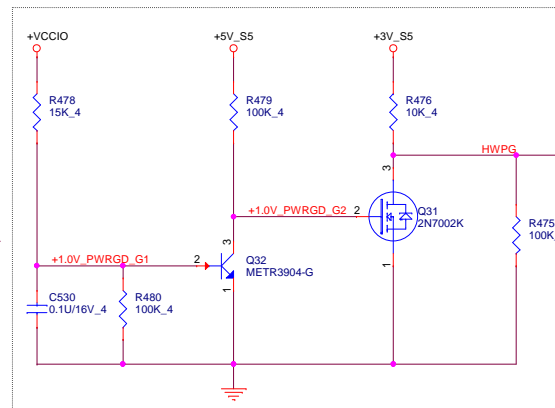
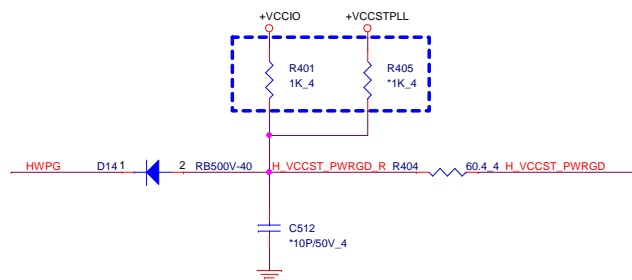


PCH Pull-high/low(CLG)

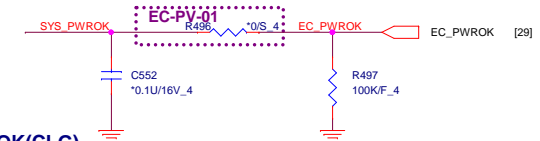


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Close to CPU side
H_VCCST_PWRGD trace 0.3" - 1.5"



System PWR_OK(CLG)

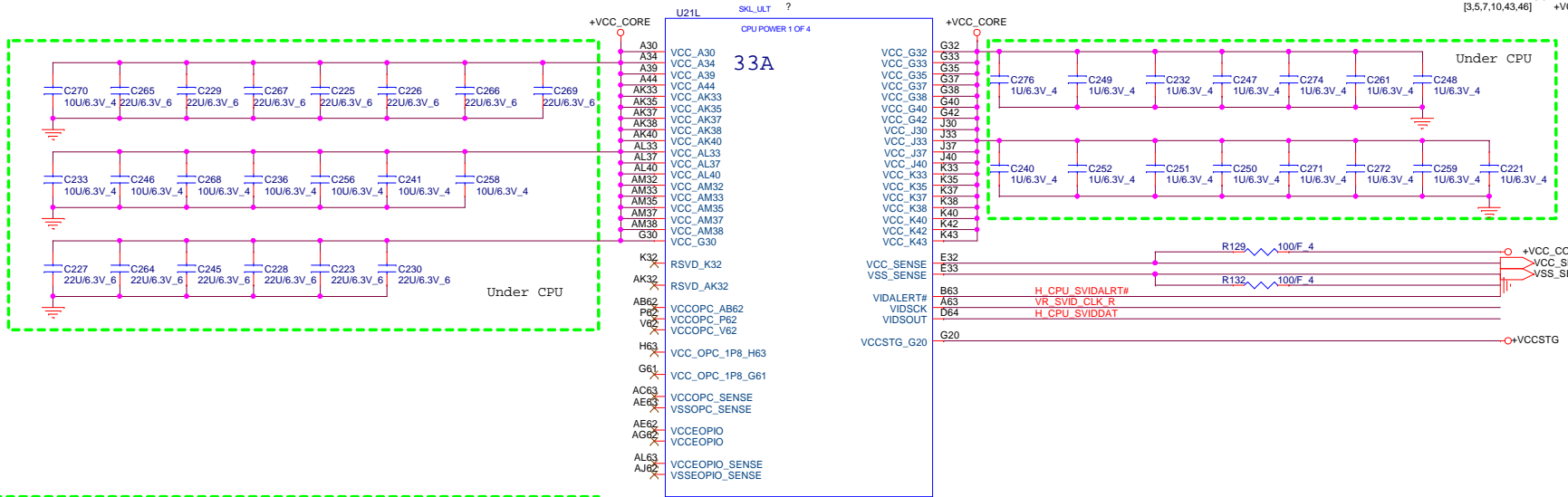


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PROJECT: HP-Hawaii

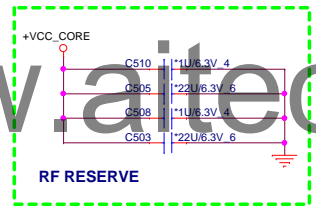
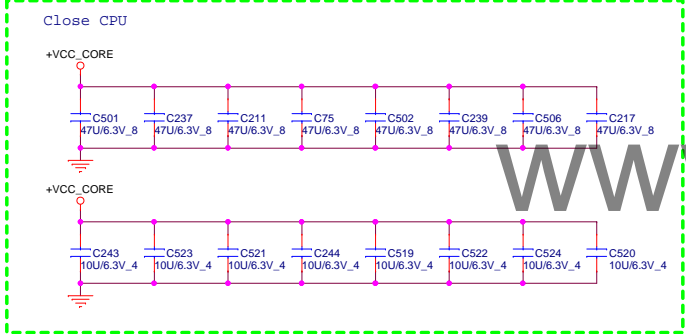
Size Custom Document Number SKL CPU Power Management Rev 1A
Date: Wednesday, March 09, 2016 Sheet 5 of 58

[32,43,44] +VCC_CORE [7] +VCCSTG [3,5,7,10,43,46] +VCCSTPLL



100- ±1% pull-up to VCC near processor.

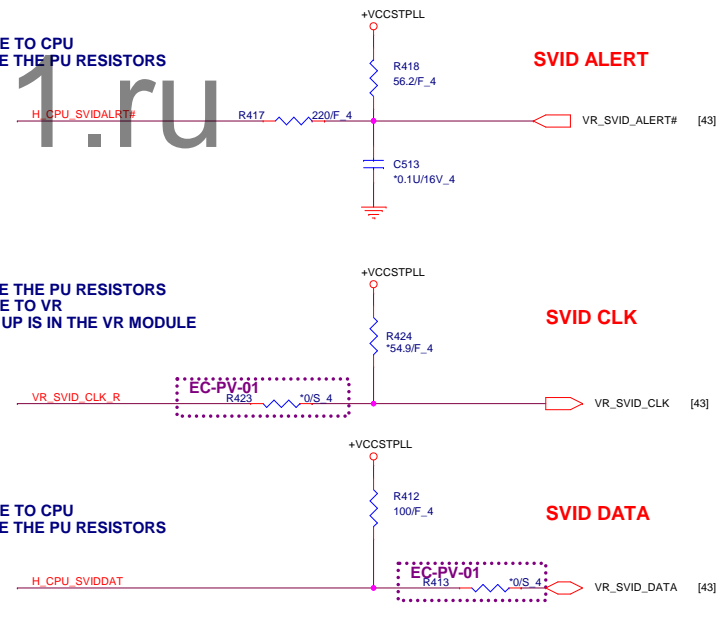
Layout note: need routing together and ALERT need between CLK and DATA.



CLOSE TO CPU
PLACE THE PU RESISTORS

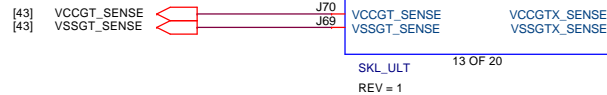
PLACE THE PU RESISTORS
CLOSE TO VR
PULL UP IS IN THE VR MODULE

CLOSE TO CPU
PLACE THE PU RESISTORS



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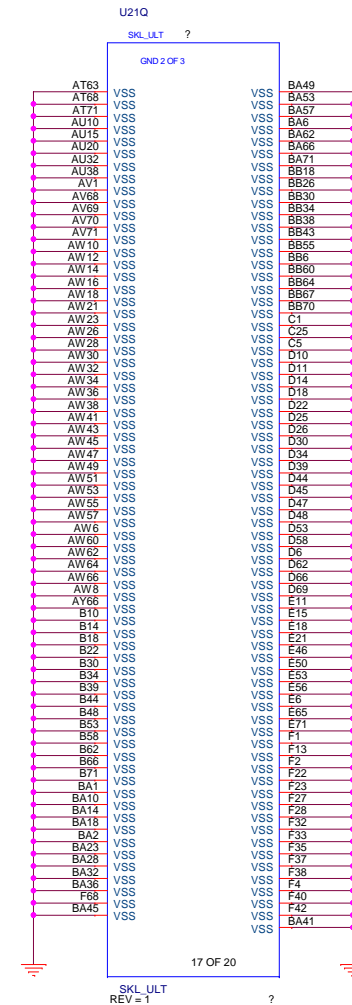
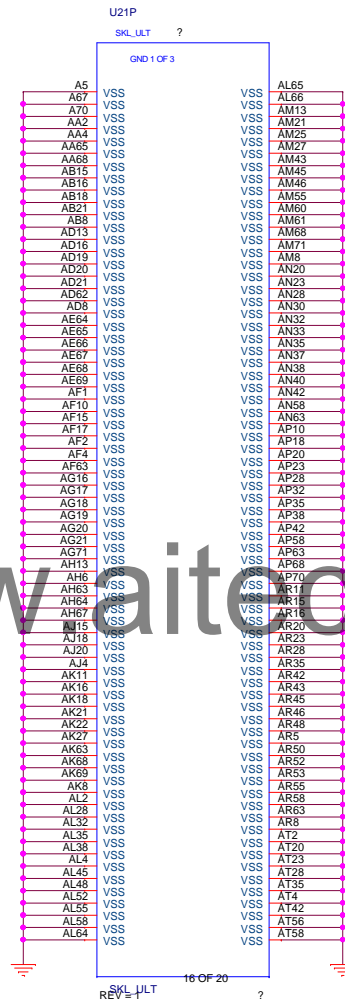
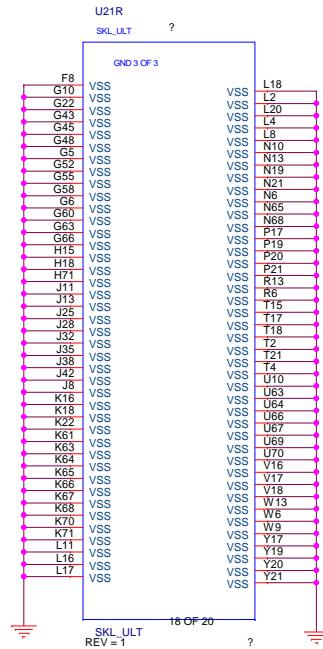


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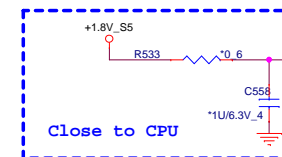
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Size
CustomDocument Number
SKL CPU GNDRev
1A

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Placement are required for future platform compatibility purpose only.

EC-PV-01
R511 *0/S 4

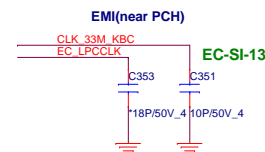
EC-PV-01
R399 *0/S 4

R407 *100K 4 +VCCSTR1

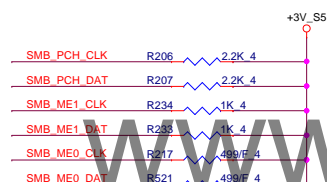
PROCESSOR Strapping			
	1	0	Circuit
CFG3 (Physical Debug Enable) DFX_Privacy	Disable:	Enable: Set DFX Enable in DFX interface MSR	
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP	

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Size Custom	Document Number SKL CPU RSVD	Rev 1
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SERIRQ	R516	10K	4
CLKRUN#	R503	8.2K/F	4
SIO_EXT_SMI#	R525	10K	4
EC_RCIN#	R495	10K	4
PCI_SERR#	R512	10K	4



EC-PV-01

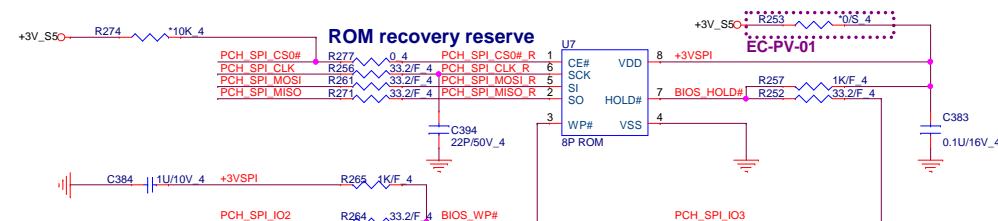
EC

EC_SPL_CS0# [29]
 EC_SPL_CLK [29]
 EC_SPL_MOSI [29]
 EC_SPL_MISO [29]
 TP36
 TP32

ROM recovery

PCH_SPL_CS0# [31]
 PCH_SPL_CLK [31]
 PCH_SPL_MOSI [17,31]
 PCH_SPL_MISO [31]
 PCH_SPL_IO2 [17,31]
 PCH_SPL_IO3 [31]

**XDP
SODIMM**



Vender	Size	P/N
Winbond	8MB	AKE3EFP0N07 (W25Q64FVSSIQ)
GD	8MB	AKE2EZ0Q000 (GD25B64CSIGR)
Socket		DFHS08FS023

TP39	←	PCH_SPI_CS0#_R	PCH_SPI_CS0#_R [31]
TP34	←	PCH_SPI_CLK_R	
TP35	←	PCH_SPI_MOSI_R	
TP38	←	PCH_SPI_MISO_R	
TP37	←	BIOS_WP#	
TP33	←	BIOS_HOLD#	

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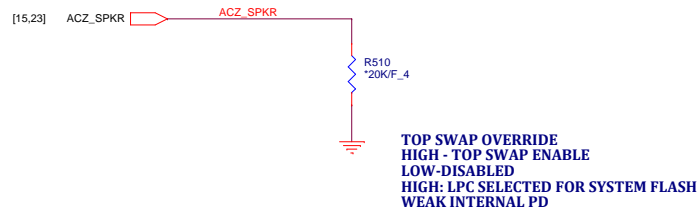
PROJECT: HP-Hawaii

Size	Document Number
Custom	SKL CPU SPI/LPC/SMB

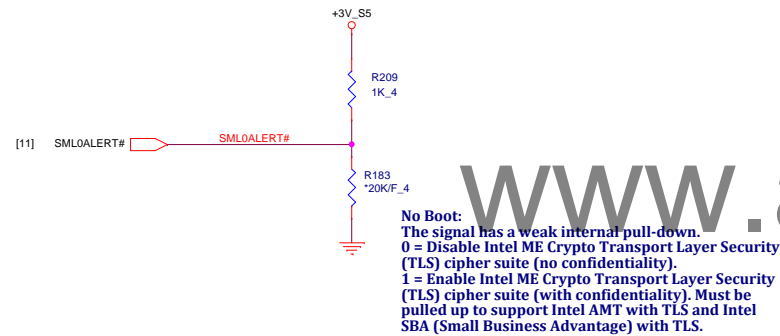
Rev

Functional Strap Definitions

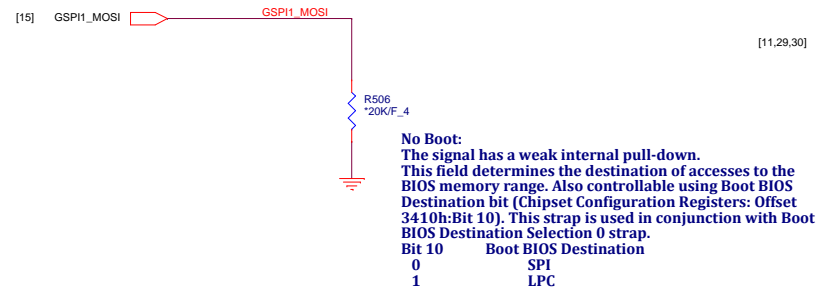
DESIGN NOTE:
WEAK PULL UP RESISTOR PRESENT ON THIS NET



No Boot:
The signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. This function is useful when running ITP/XDP.



No Boot:
The signal has a weak internal pull-down.
0 = Disable No Reboot mode.
1 = Enable No Reboot mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

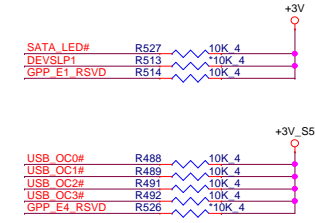
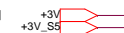


No Boot:
The signal has a weak internal pull-down.
0 = LPC is selected for EC.
1 = eSPI is selected for EC.

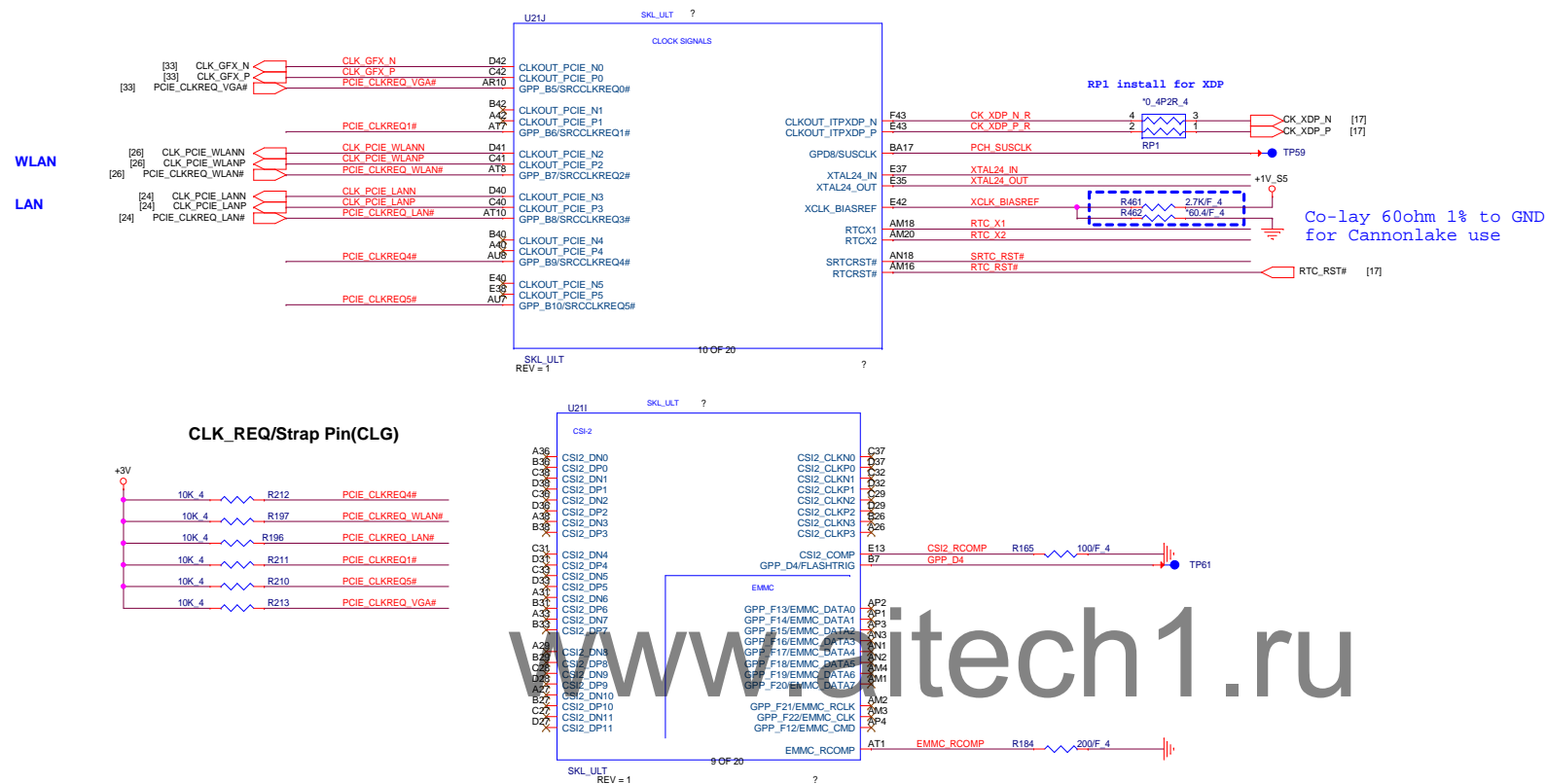
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PROJECT: HP-Hawaii

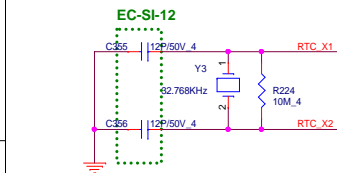
Size Custom	Document Number SKL CPU Strap	Rev. 1A
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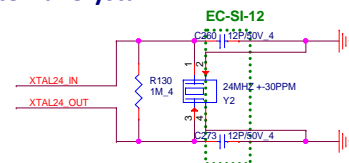
USB2.0	Function
PORT-1	USB3 COMBO1
PORT-2	Cardreader
PORT-3	Camera
PORT-4	USB3 COMBO2
PORT-5	BT
PORT-6	NC
PORT-7	USB2 PORT1
PORT-8	USB2 PORT2
PORT-9	Touch Panel
PORT-10	NC



RTC Clock 32.768KHz

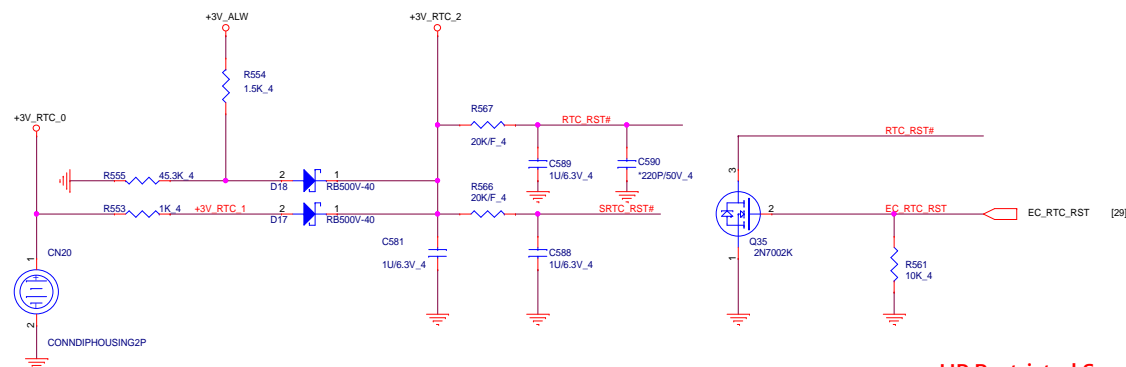


External Crystal

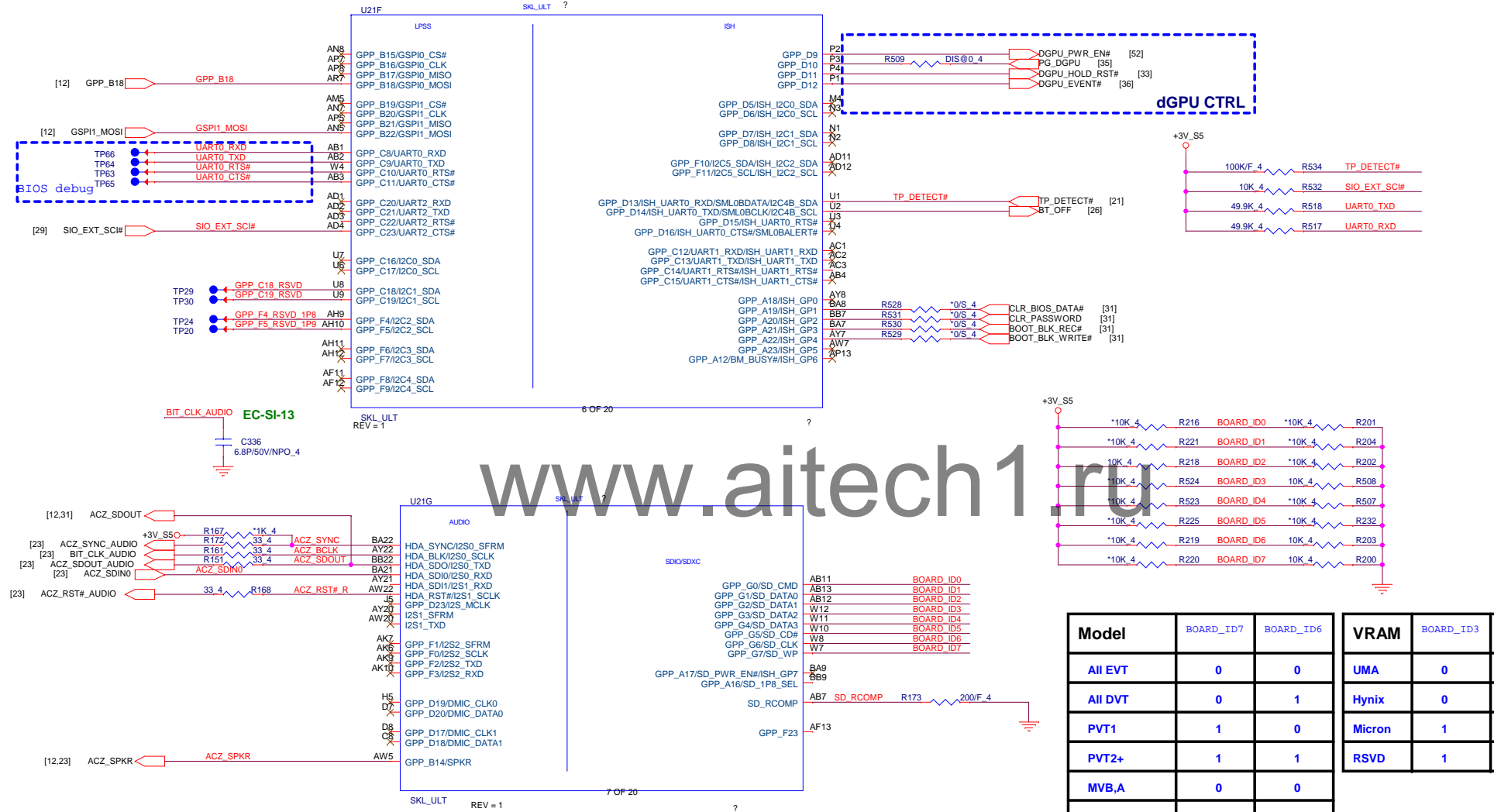


RTC Circuitry(RTC)

RTC Power trace width 20mils.

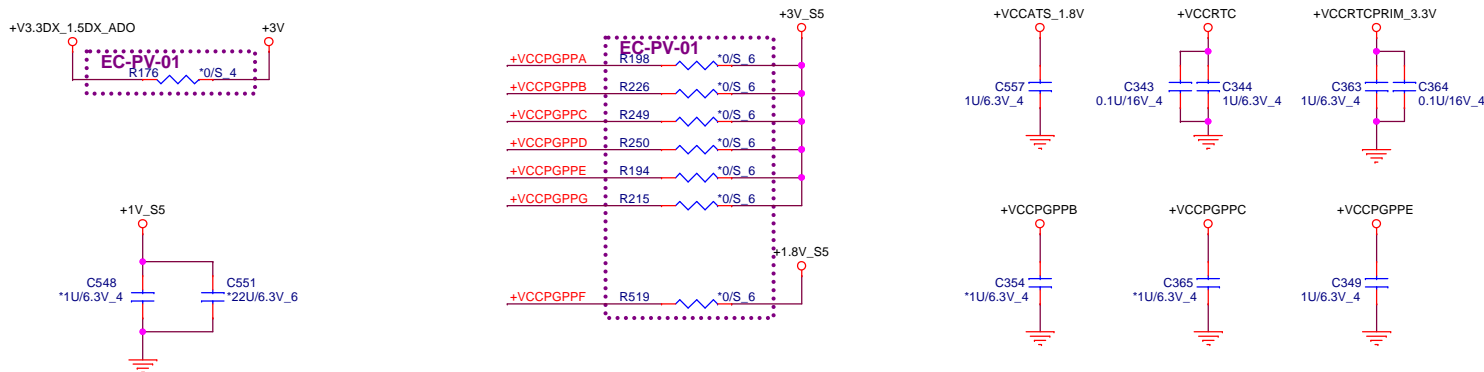
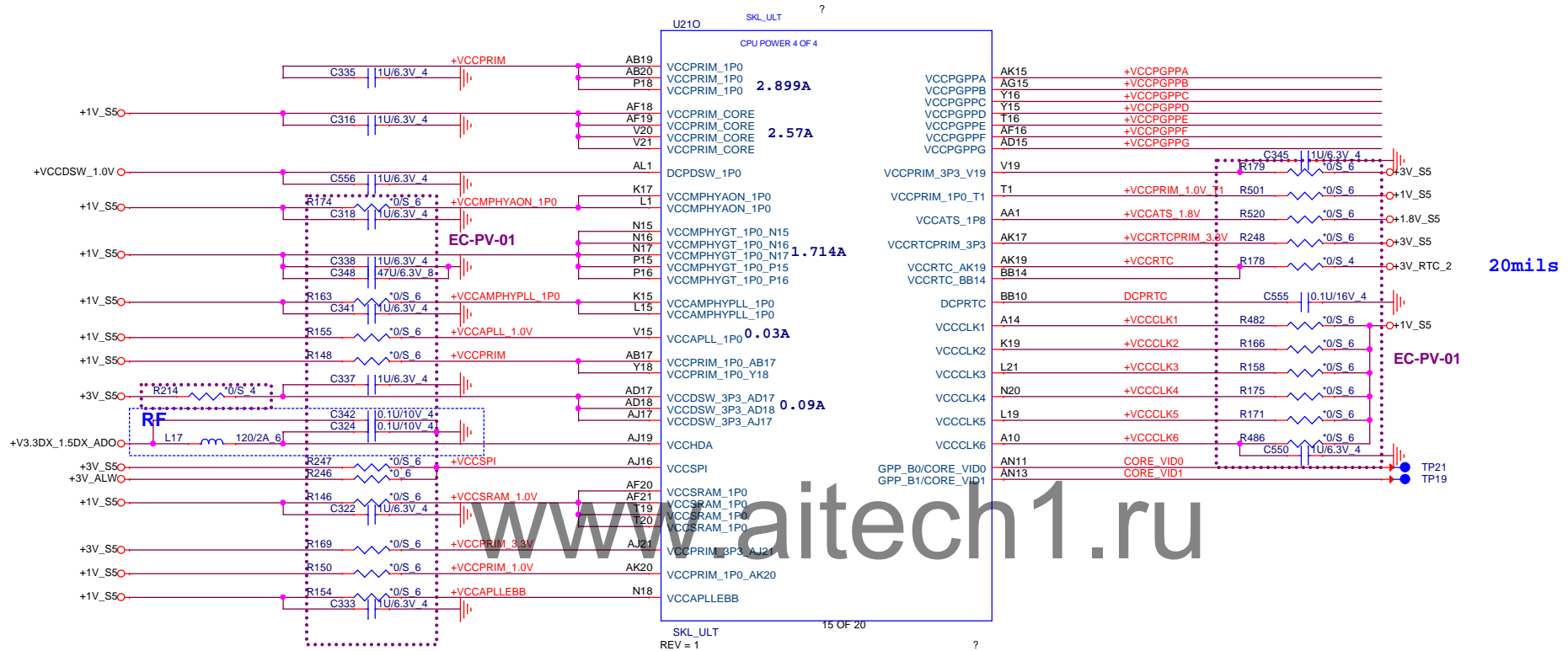


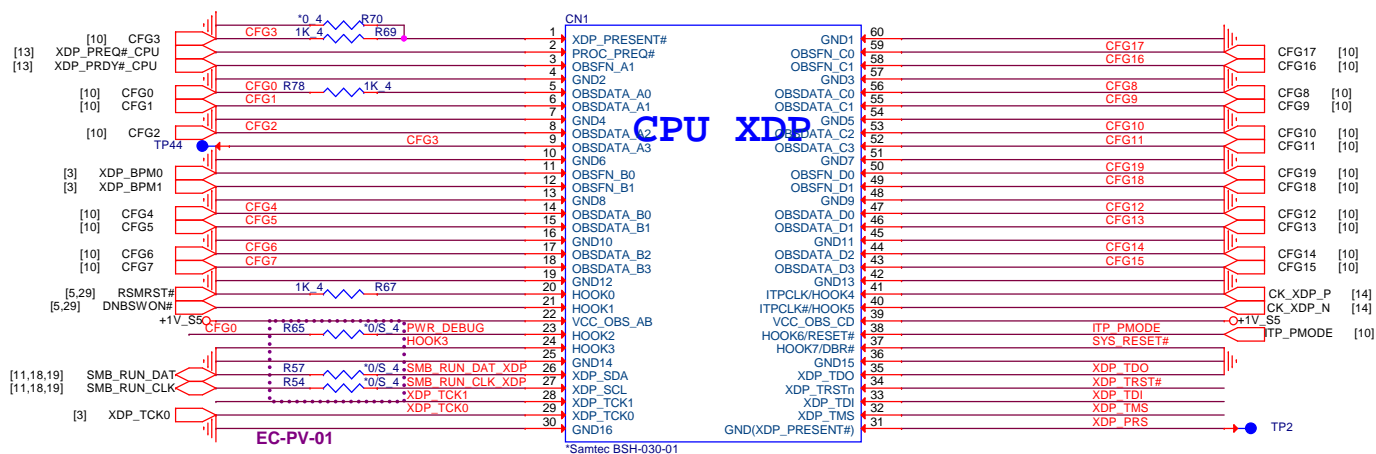
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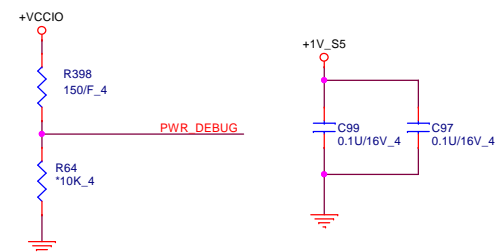
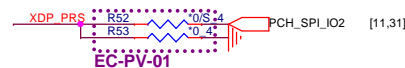
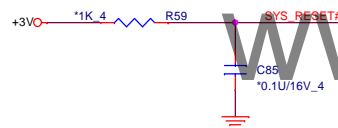
Model	BOARD_ID7	BOARD_ID6	VRAM	BOARD_ID3	BOARD_ID2
All EVT	0	0	UMA	0	0
All DVT	0	1	Hynix	0	1
PVT1	1	0	Micron	1	0
PVT2+	1	1	RSVD	1	1
MVB,A	0	0			
1st Major ECN	0	1			
2nd Major ECN	1	0			
3rd Major ECN	1	1			

[10,14,17,41,46,48] +1V_S5
[10,29,42,46,48] +1.8V_S5
[5,11,12,13,15,17,18,21,24,26,29,31,32,39,40,41,42,46,47,48,52] +3V_S5
[5,14] +3V_RTC_2
[3,5,11,12,13,14,17,18,19,20,21,22,24,25,29,30,34,35,43,46,51,52] +3V

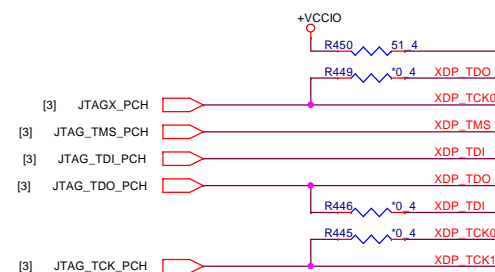
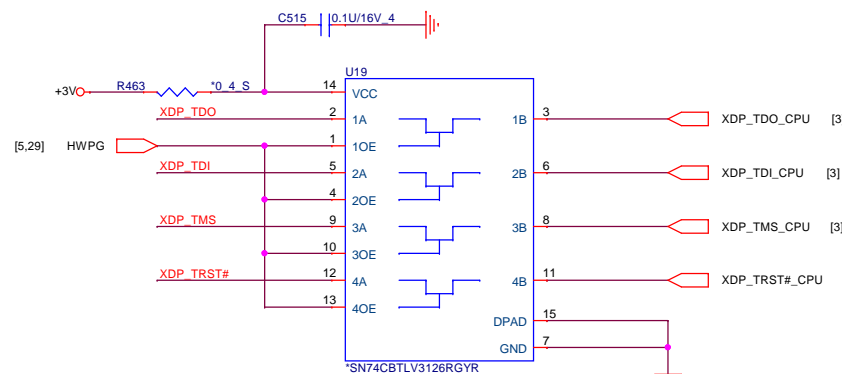
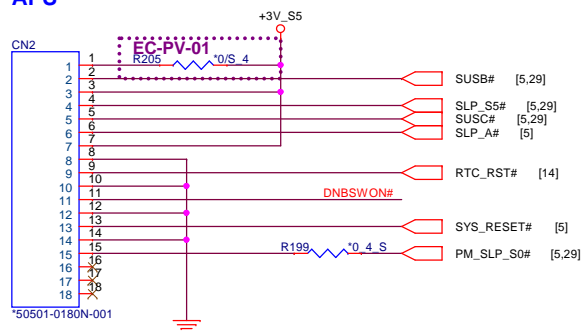




[11,31] PCH_SPI_MOSI



APS



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Size Custom Document Number SKL CPU XDP/APS

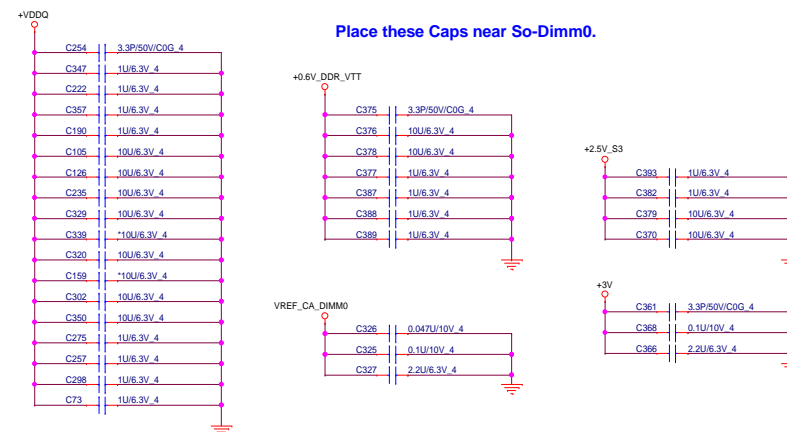
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Rev 1A



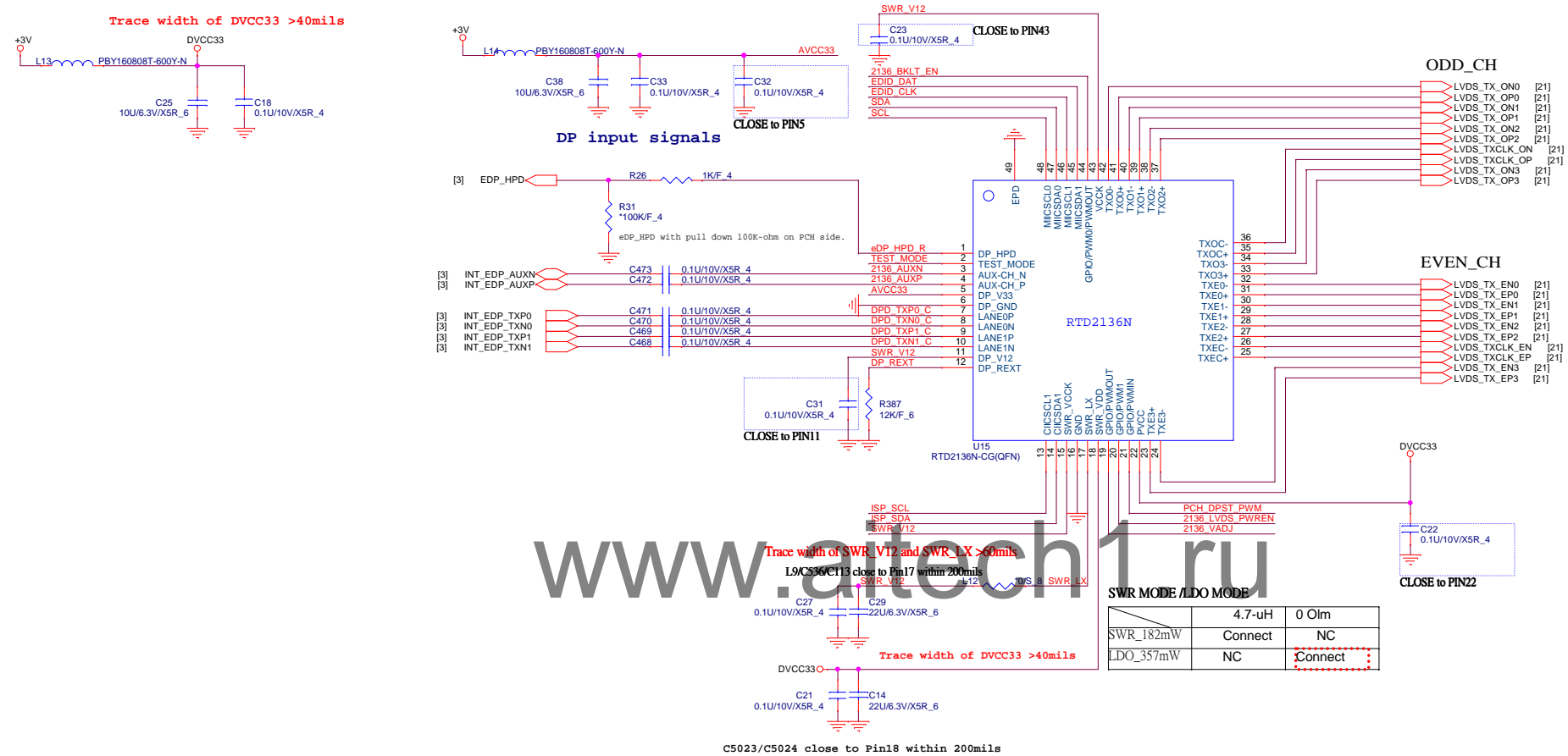
VREF CA DIMM0 Solution



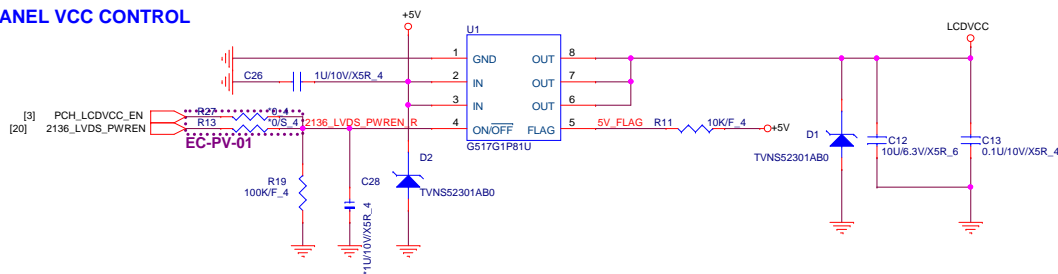
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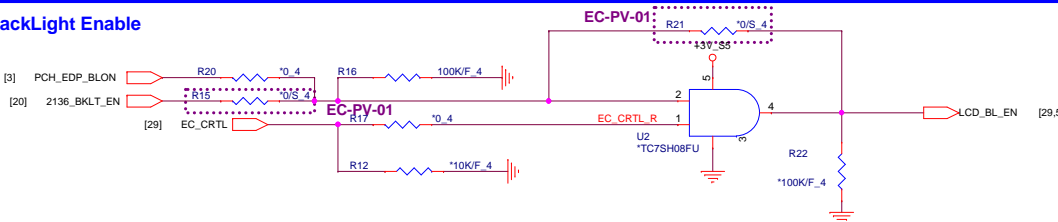
Size Custom	Document Number DDR4 SODIMM H=4	Rev 1A
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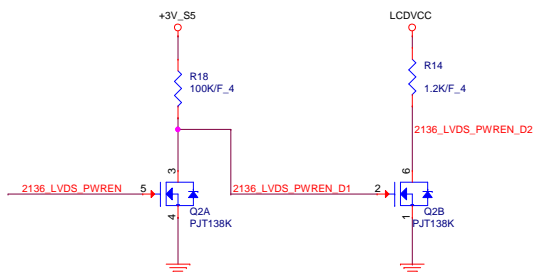
PANEL VCC CONTROL



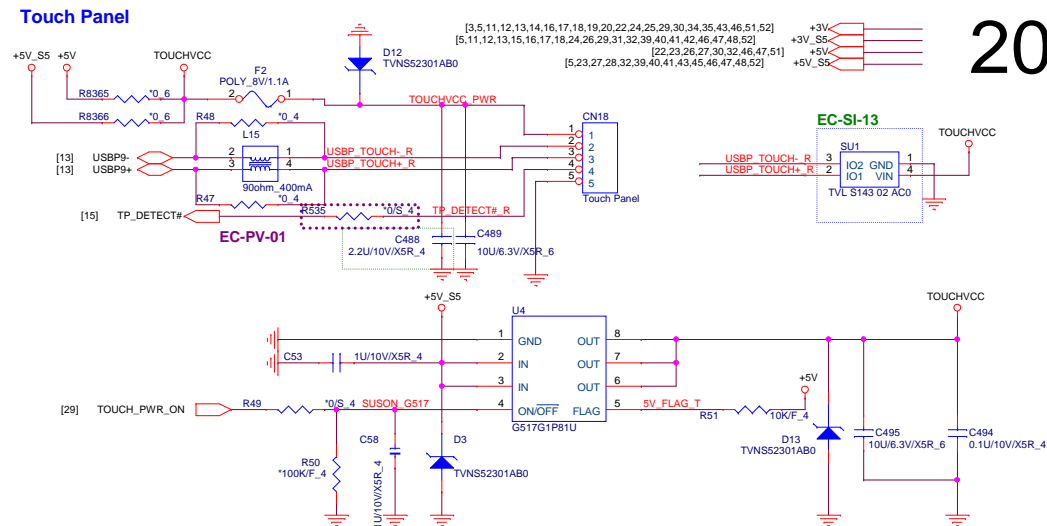
BackLight Enable



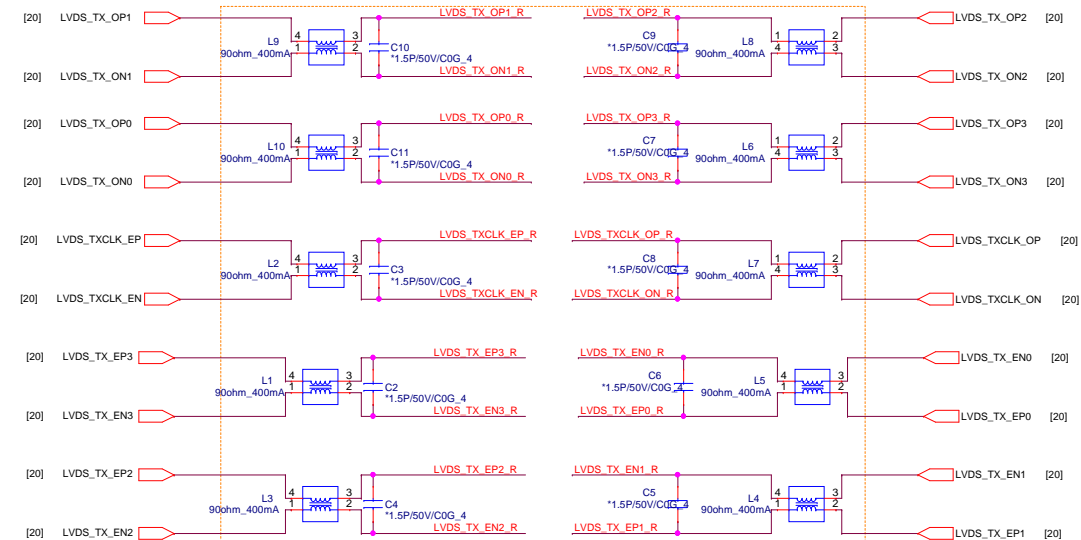
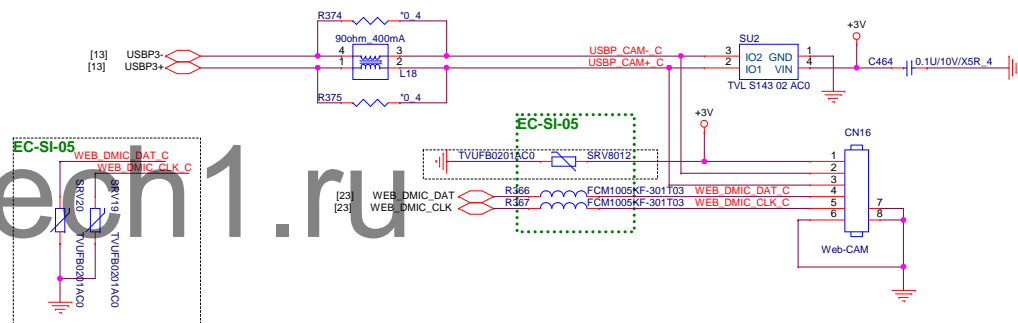
LCDVCC Discharge Circuit



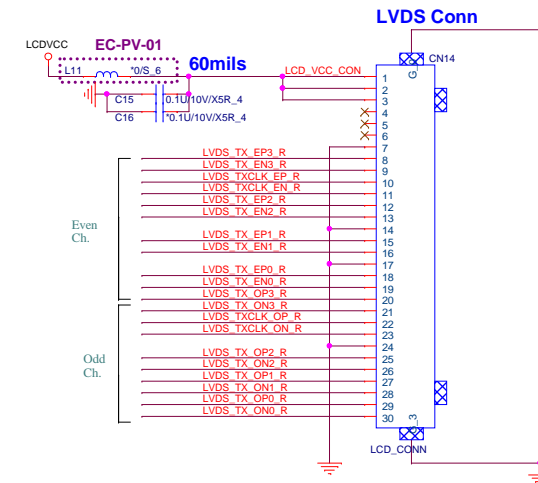
Touch Panel



CCD CONN



LVDS Conn



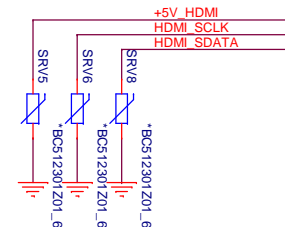
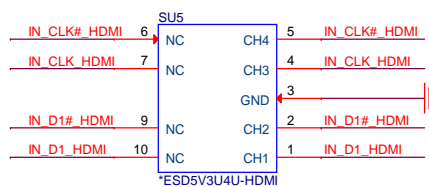
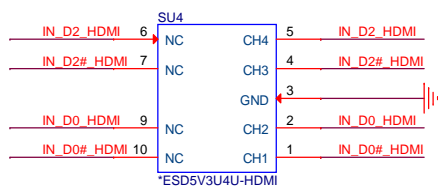
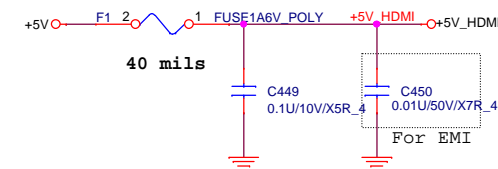
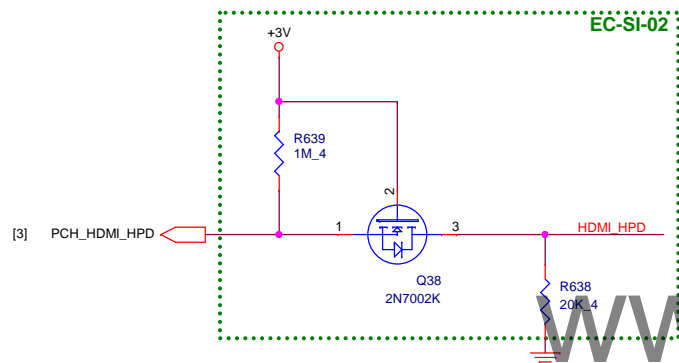
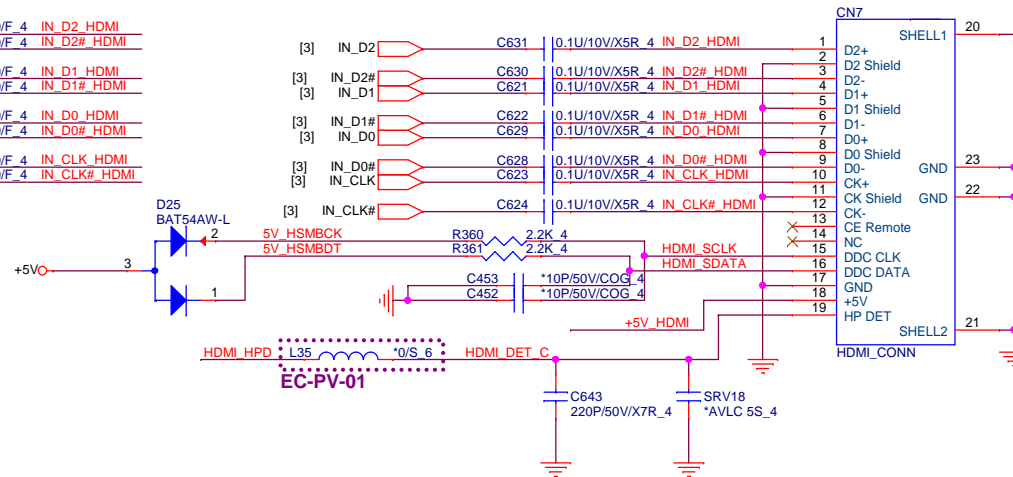
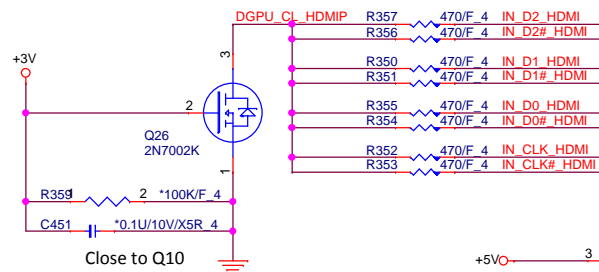
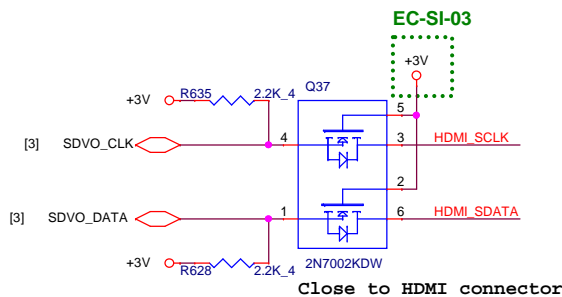
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HDMI CONN

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Layout note:Place close to HDMI Conn

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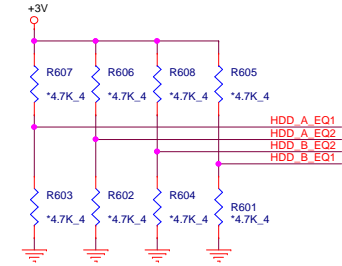
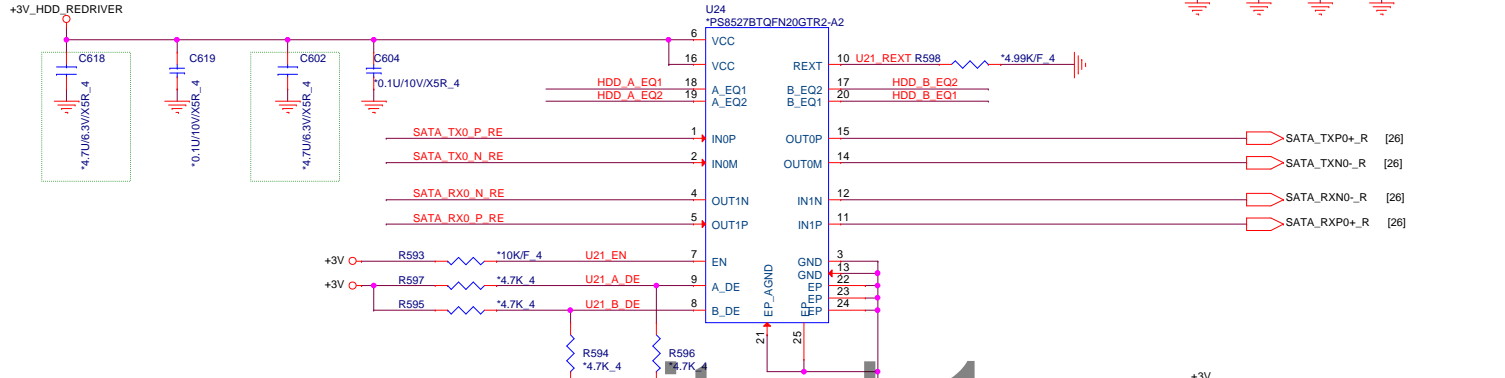
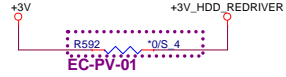
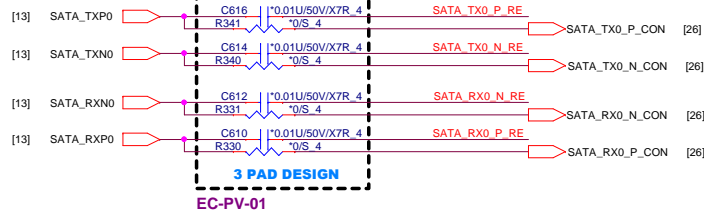
**Quanta Computer Inc.**

PROJECT: HP-Hawaii

Size Custom	Document Number HDMI	Rev 1A
Date:	Monday, February 15, 2016	Sheet 22 of 58

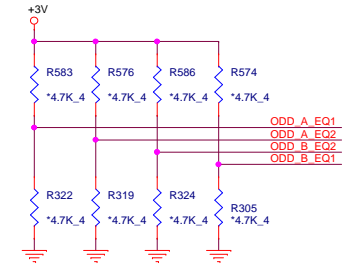
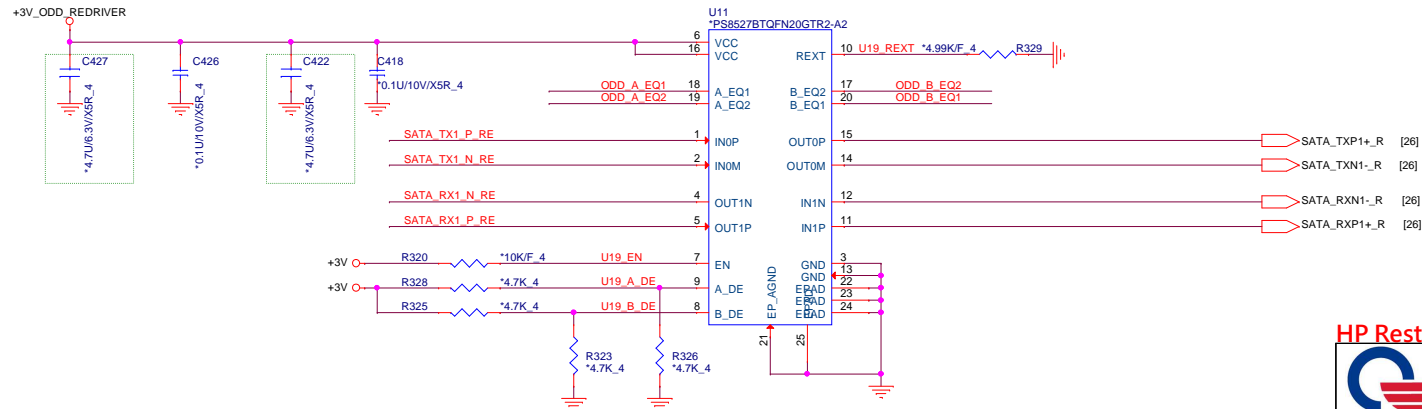
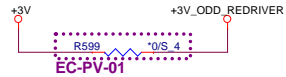
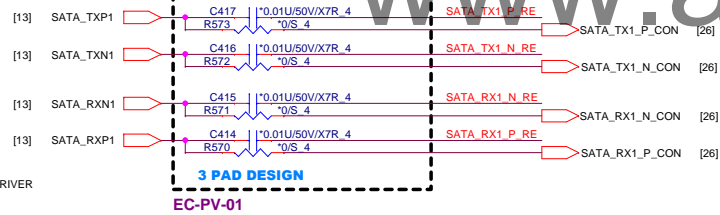
HDD REDRIVER

C44,C45,C46,C47 CLOSE TO RE-DRIVER IC

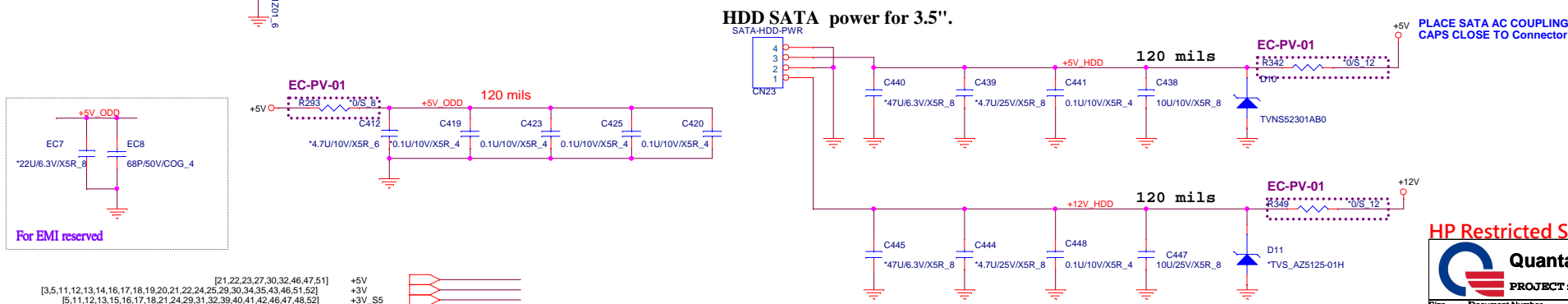
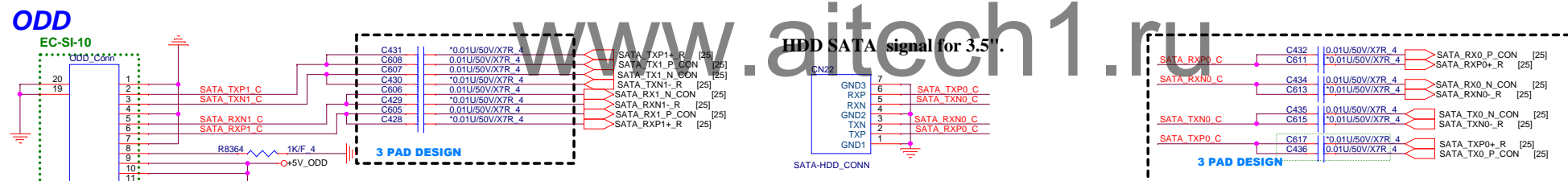
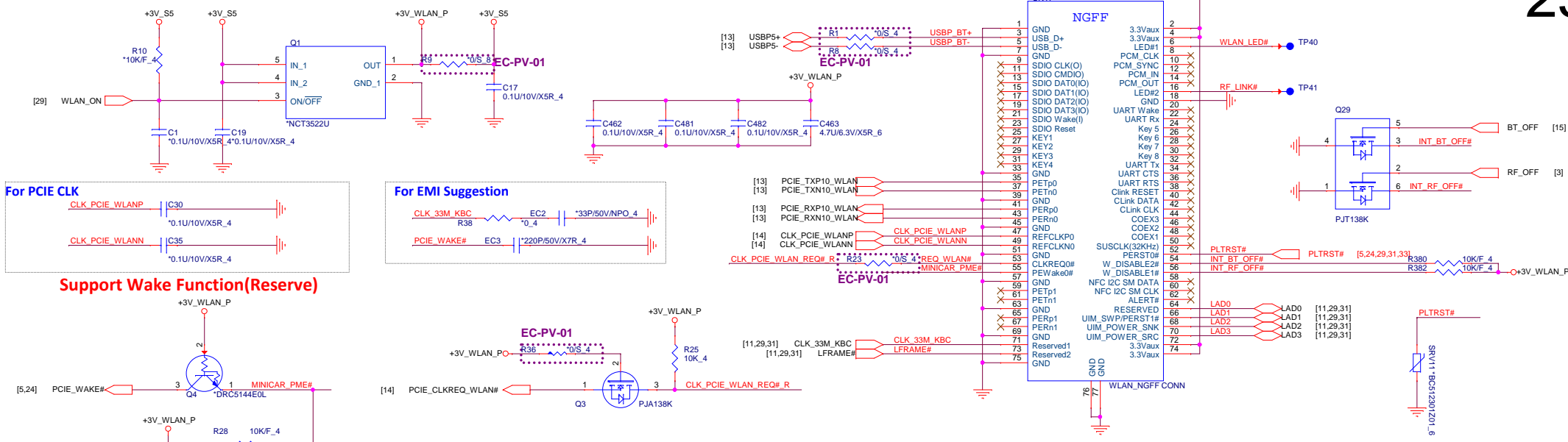


ODD REDRIVER

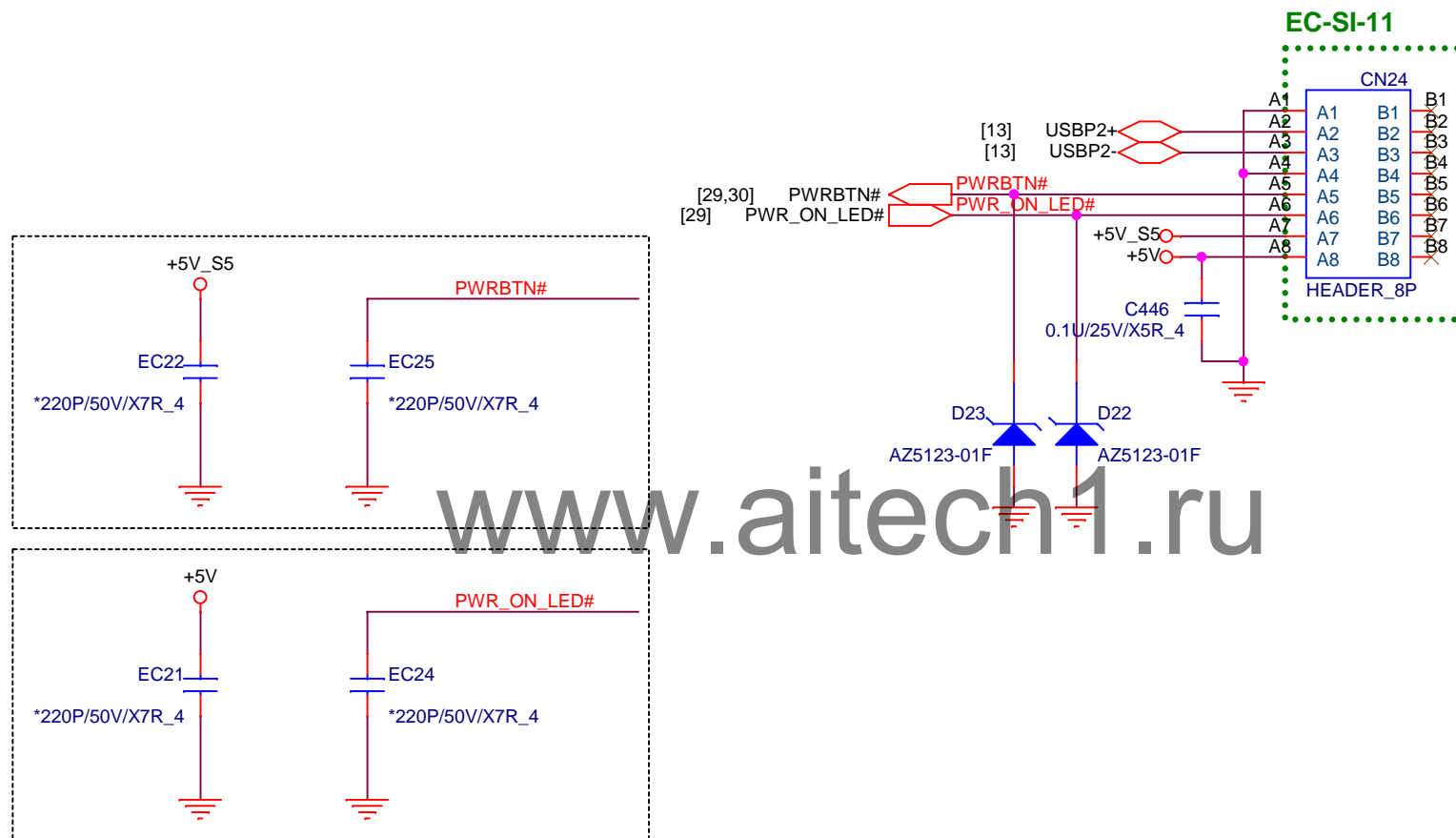
C53,C57,C58,C59 CLOSE TO RE-DRIVER IC



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Mini Card WLAN/BT(Optional) PCIe M.2_power(S5)

Card reader/Power button conn



HP Restricted Secret



Quanta Computer Inc.

PROJECT: HP-Hawaii

Size
A

Document Number

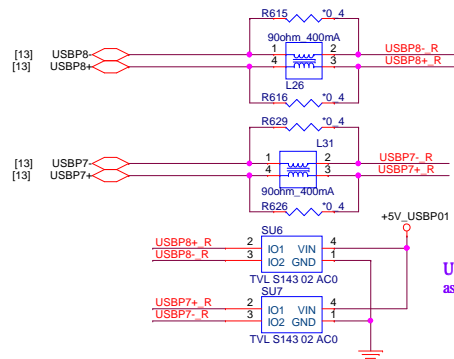
Card reader/PWR BTN CONN

Rev
1A

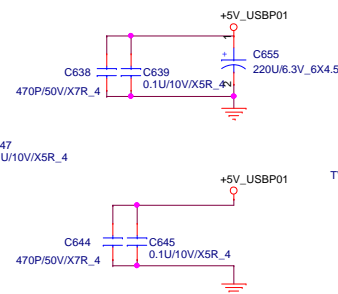
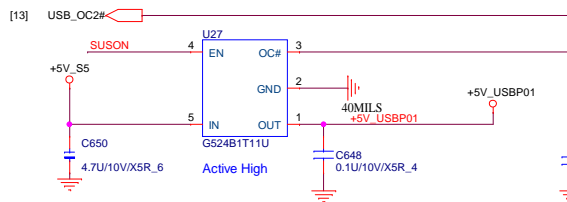
Date: Tuesday, March 08, 2016

Sheet 27 of 58

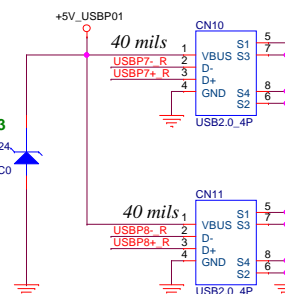
USB 2.0



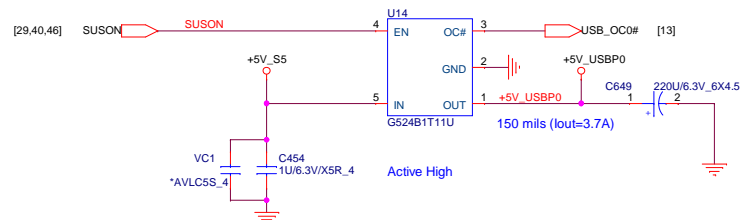
USD protection diodes for ESD.
as close as possible to USB connector pins.



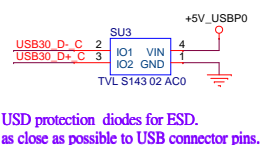
EC-S



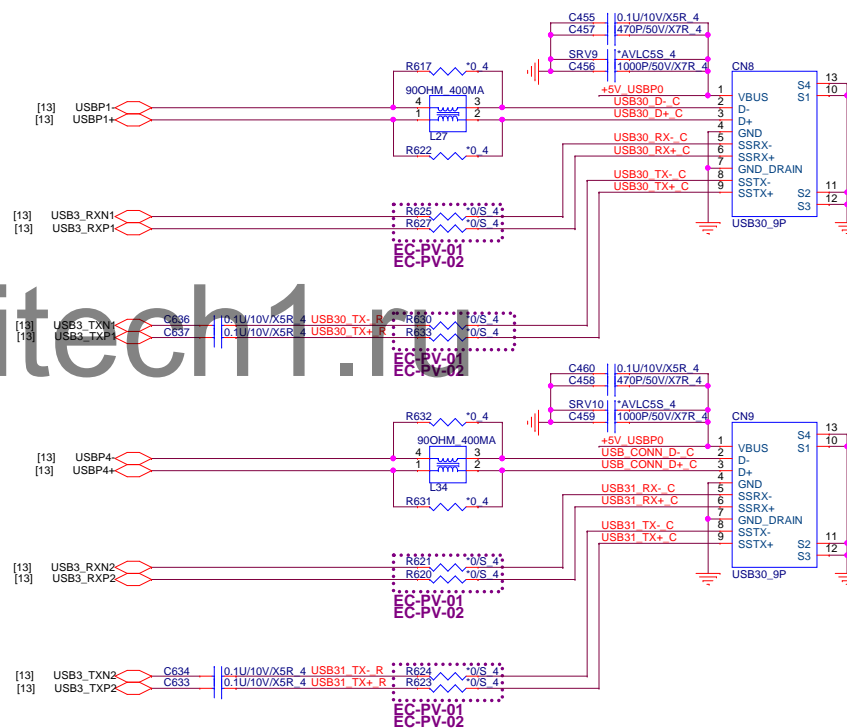
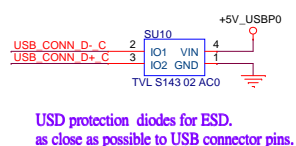
USB 2.0/3.0 Combo



For ESD



For ESD



CLR_CMOS

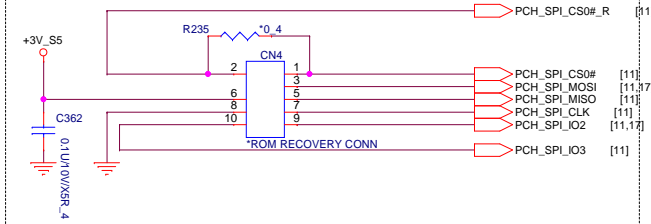
Jumper	Pre-production	Production
BOOT_BLK_Recovery	X	X
BOOT_BLK_Enable	O	X

Jumper	Type
Pop CLR BIOS_DAT	
Pop CLR PASSWD	
Pop BOOT_BLK_Recovery	
Pop BOOT_BLK_Enable	

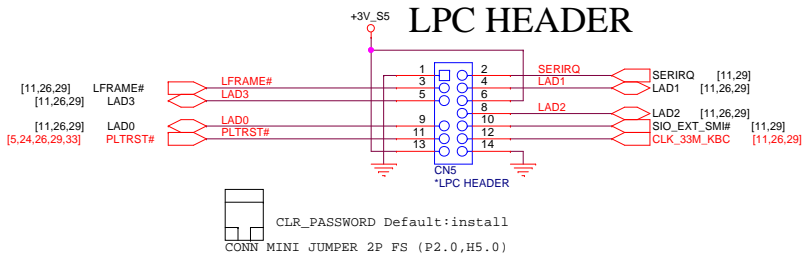


ON Chip select:Default:iinsatall (PROTO only)
CONN MINI JUMPER 2P FS (P2.0,H5.0)

ROM recovery (for pre-production only)

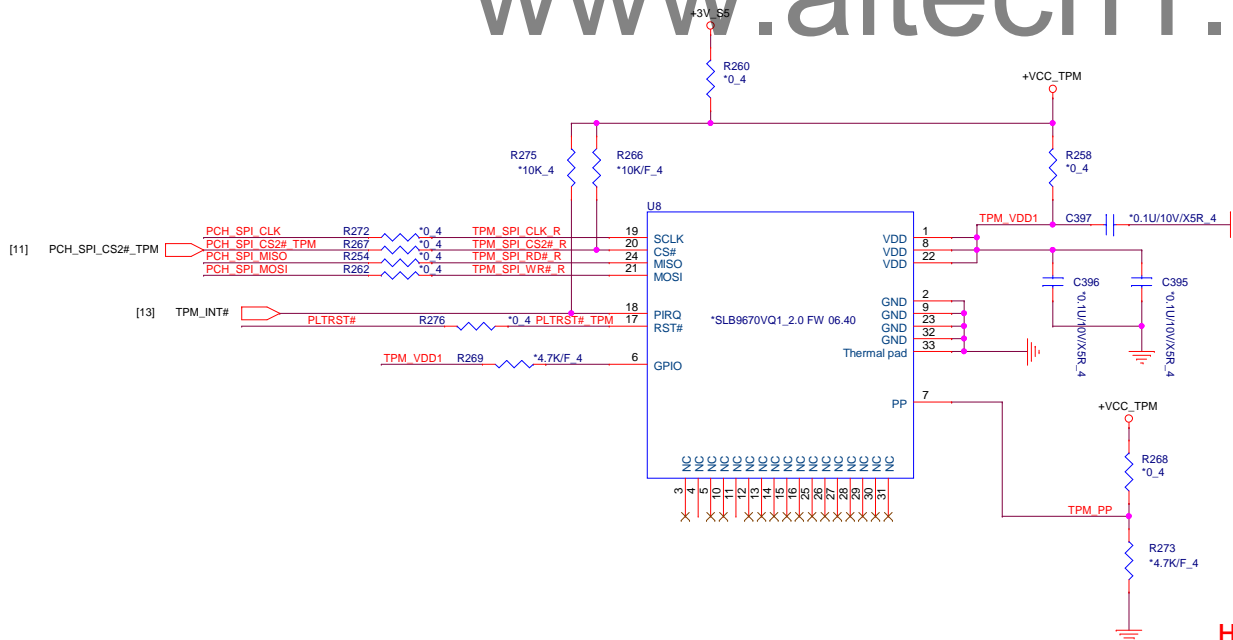


LPC HEADER



TPM (1.2 or 2.0)

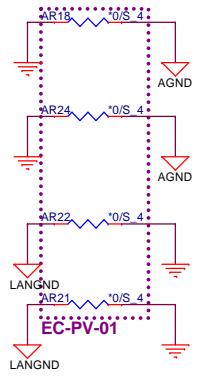
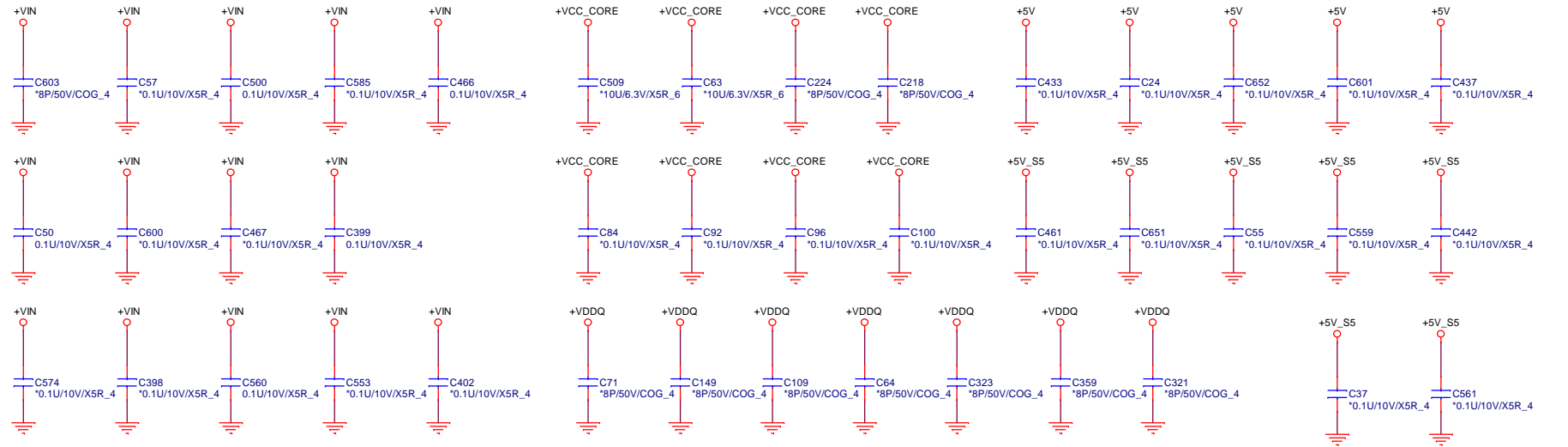
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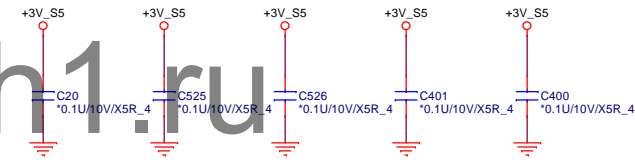
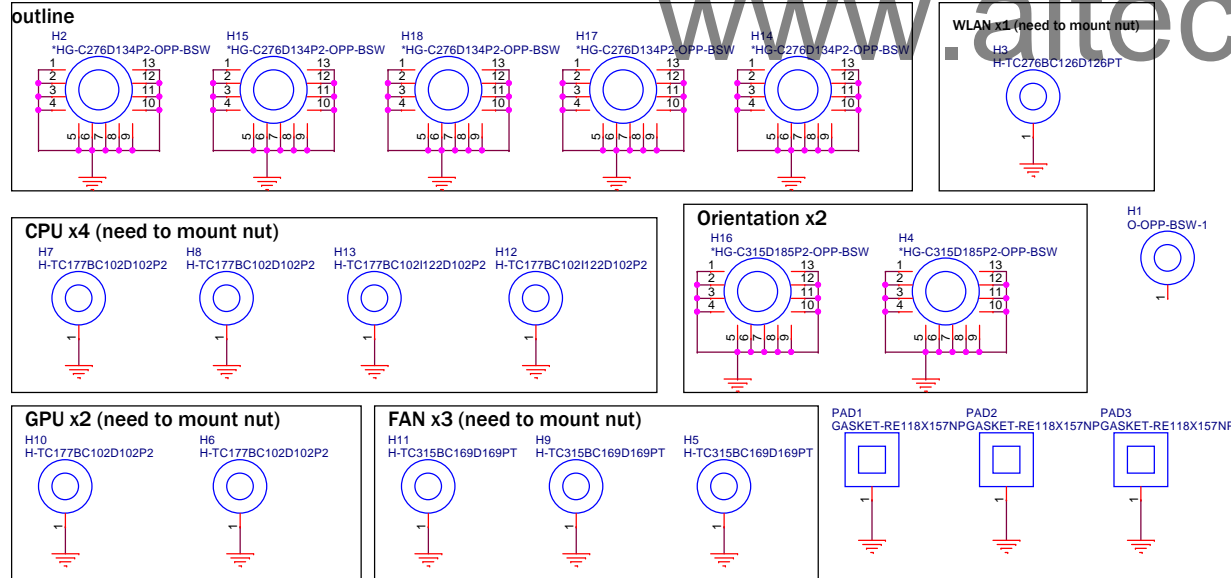
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RF/EMI Suggestion

31

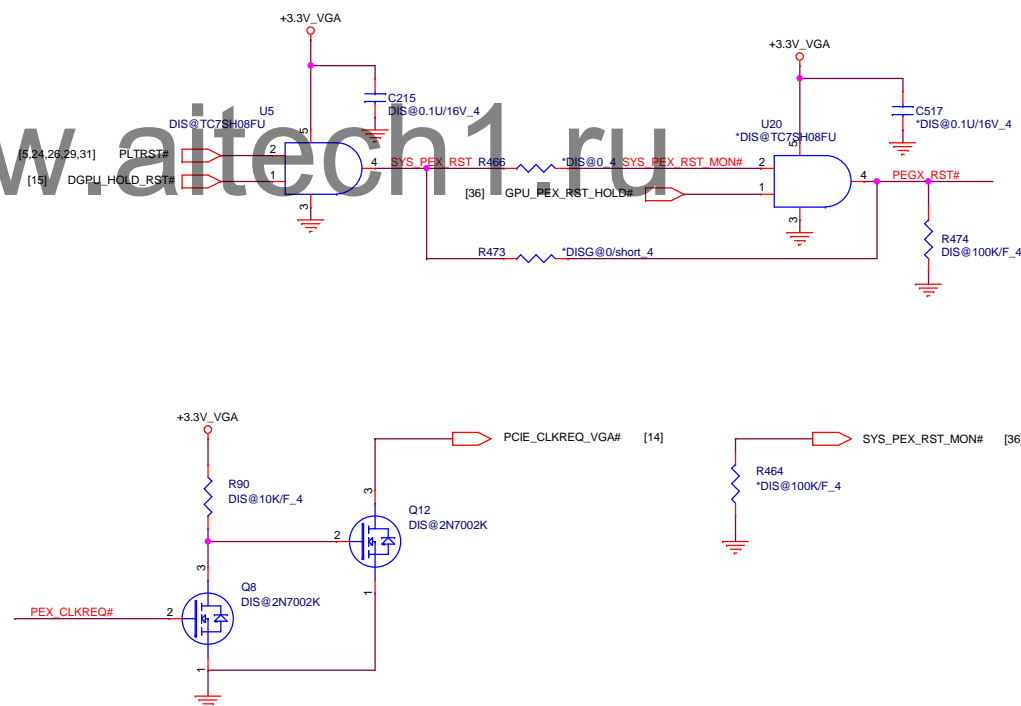
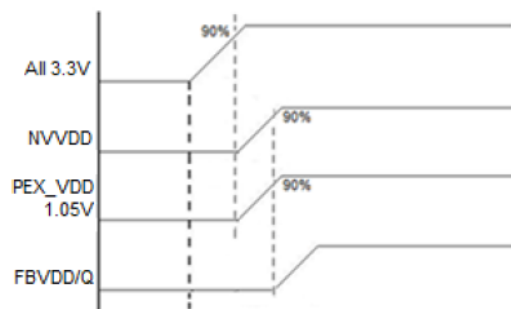
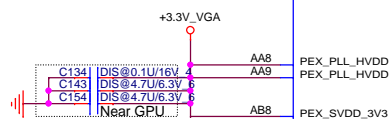


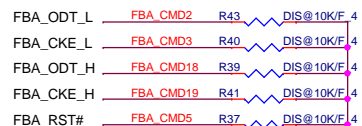
Holes



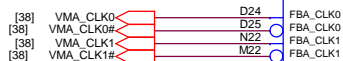
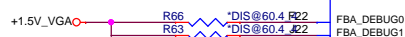
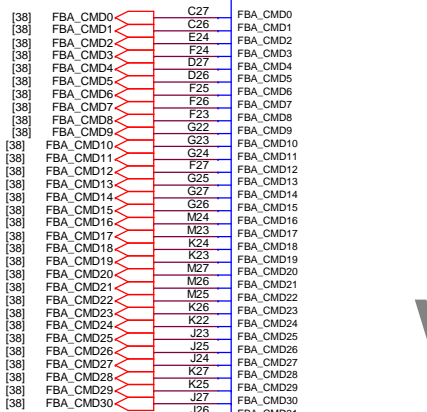
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Quanta Computer Inc.	
PROJECT: HP-Hawaii	
Size Custom	Document Number EMI/RF/Holes
Date: Thursday, March 17, 2016	Rev 1A

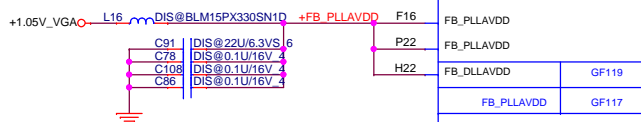




Mode D Command Mapping



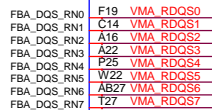
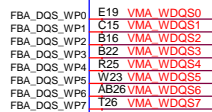
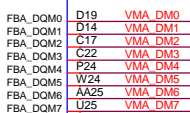
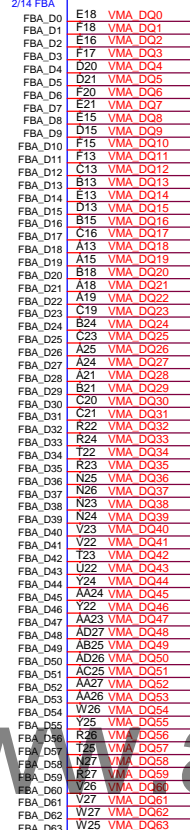
FB_PLLAVDD = 55mA



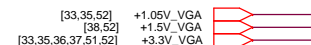
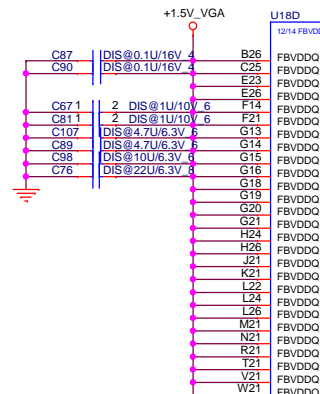
FB_DLLAVDD = 15mA



2/14 FBA

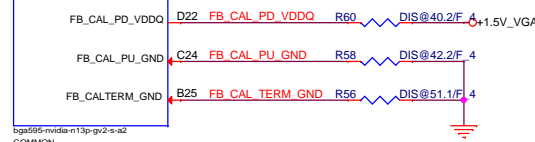
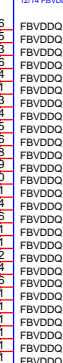


FBVDDQ + FBVDD = 3.116A



U18D

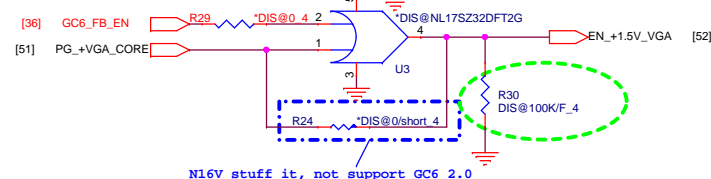
12/14 FBVDDQ



COMMON

For support GC6 2.0

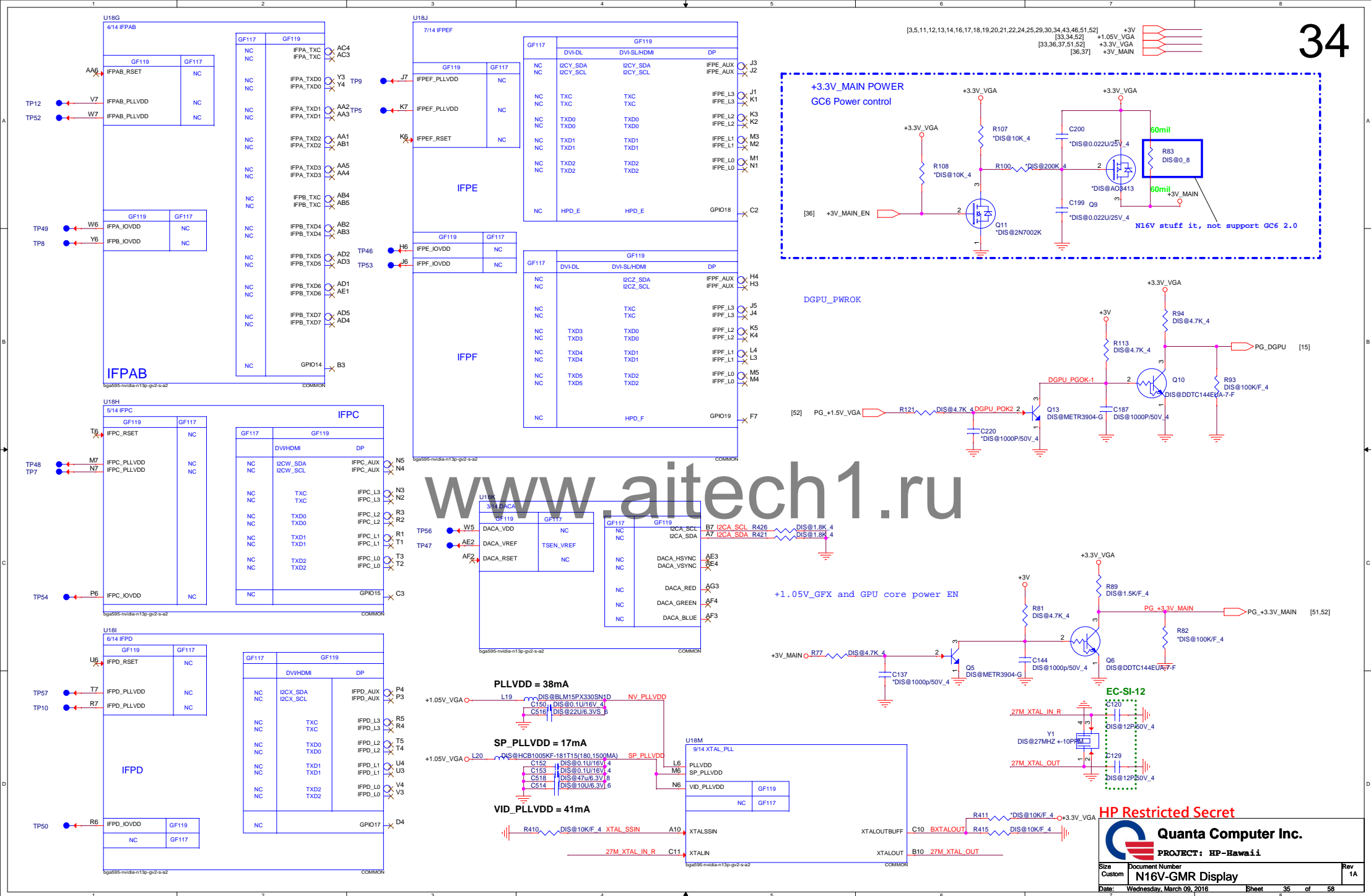
Remove GC6 1.0 for Nvidia suggest 11/27

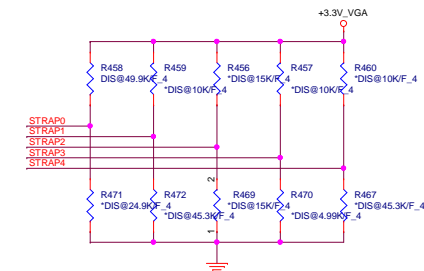
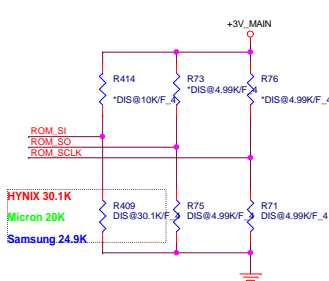
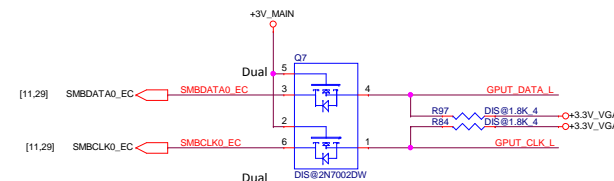


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Quanta Computer Inc.
 PROJECT: HP-Hawaii

Size Custom Document Number N16V-GMR Memory Rev 1A
 Date: Wednesday, March 09, 2016 Sheet 34 of 58





```

ROM_SCLK = Stuff 4.99K pull down
ROM_SO   = Stuff 4.99K pull down
STRAP0   = Stuff 49.9K pull up
STRAP1   = NC
STRAP2   = NC
STRAP3   = NC
STRAP4   = NC
ROM_SI   = VRAM Configuration follow below table

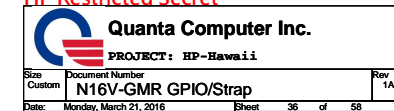
```

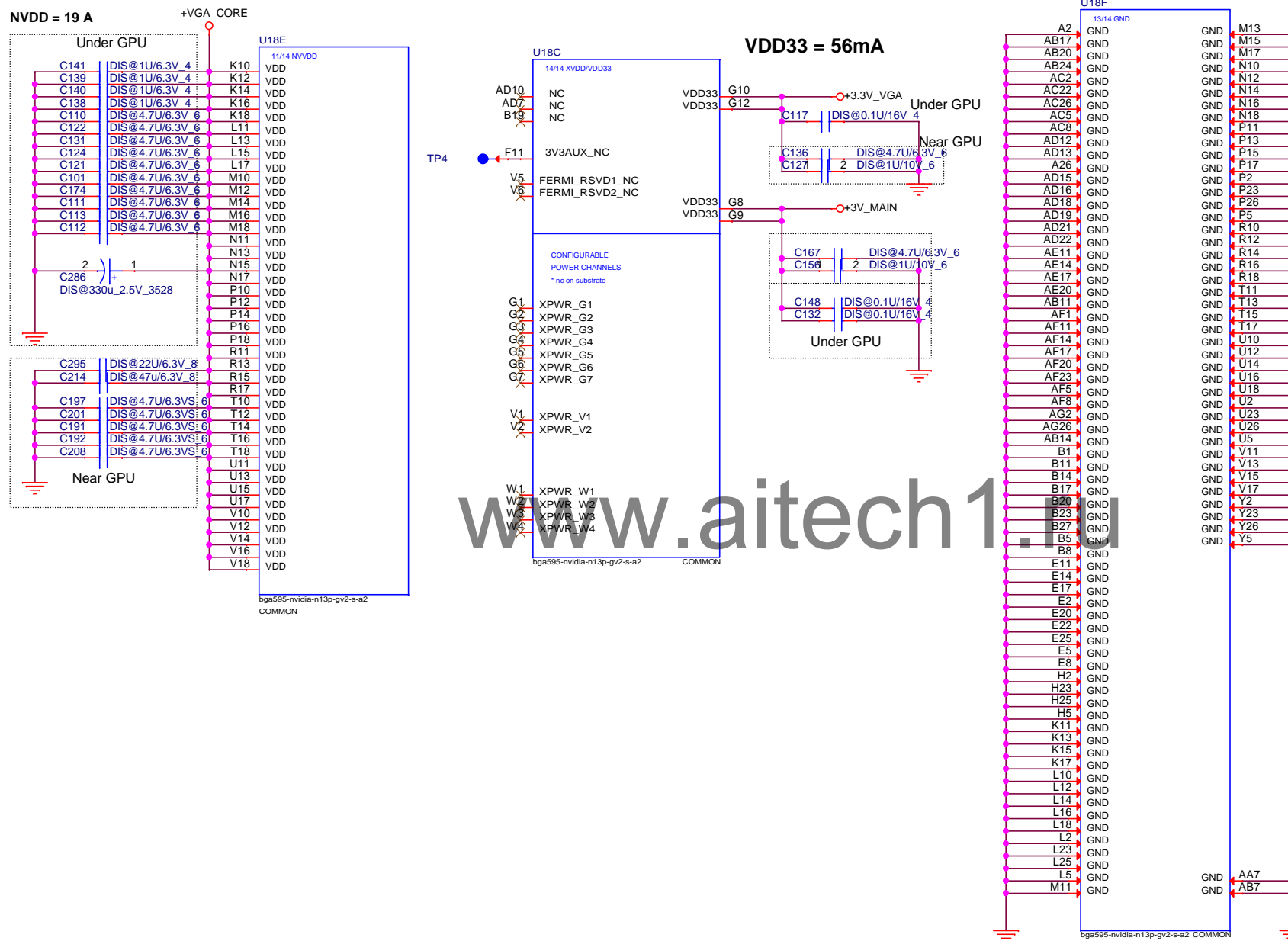
	PU-VDD	PD	QCI P/N
4.99K	1000	0000	CS24992FB28
10K	1001	0001	CS31002FB26
15K	1010	0010	CS31502FB24
20K	1011	0011	CS32002FB29
24.9K	1100	0100	CS32492FB16
30.1K	1101	0101	CS33012FB18
34.8K	1110	0110	CS33482FB06
45.3K	1111	0111	CS34532FB18

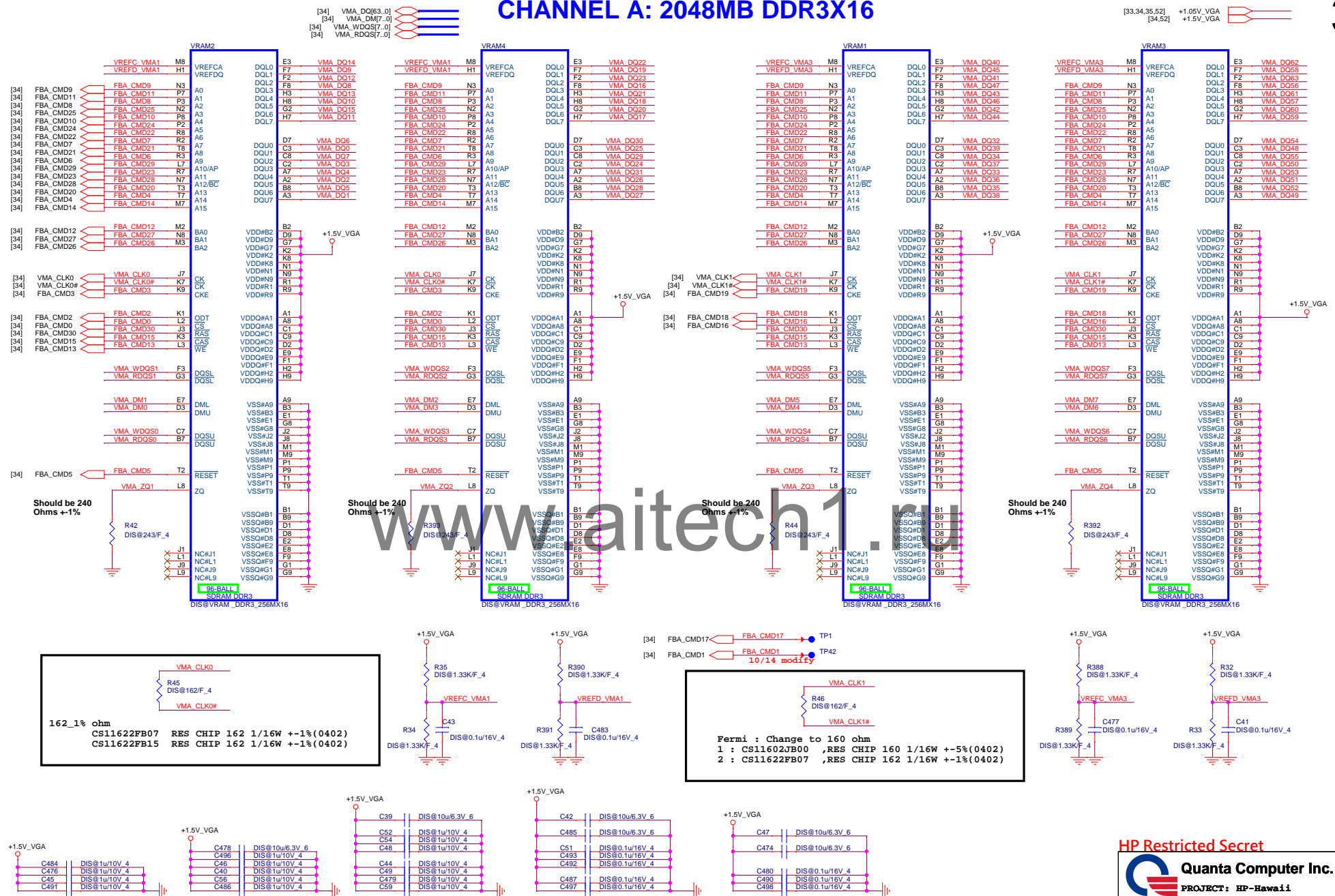
GPIO	I/O	PIN	USAGE
0	IN	FB_CLAMP_MON	FB Clamp monitor (GC6 1.0)
0	OUT	GC6_FB_EN	GC6 FB Enable (GC6 2.0)
5	OUT	+3V_MAIN_EN	Enable GC6 +3V_MAIN
6	OUT	FB_CLAMP_REQ#	Active low FB Clamp toggle request (GC6 1.0)
6	IN	DGPU_EVENT#	DGPU EVENT from CPU (GC6 2.0)
8	OUT	VGA_OVT#	ACTIVE LOW THERMAL OVER TEMP
9	OUT	ALERT	ACTIVE LOW THERMAL ALERT
11	OUT	PWR_VID	GPU CORE_VDD PWM Control signal
12	IN	PWR_LEVEL	AC Power detect or power supply overdraw input
13	OUT	PSI	Phase Shedding

RAMCFG [3:0]	DESCRIPTION	1.5V_DDR3	Vendor	Vendor P/N	ROM_SI	STN_B/S	Configuration
	256Mx16						
0011	DDR3 256Mx16, 64bit, 4Gb, 1000MHz		Micron	MT41J256M16L1Y-091G:N	PD 20K ohm	AKD59GSTL02	Single Rank or
1001	DDR3 256Mx16, 64bit, 4Gb, 1000MHz		HYNIX	H5TC4G63CFR-N0C	PD 30.1K ohm	AKD5PZDTW03	Single Rank stuffing
1000	DDR3 256Mx16, 64bit, 4Gb, 1000MHz		Samsung	K4W4G1646E-BC1A	PD 24.9K ohm	AKD5PGDT502	for Dual Rank

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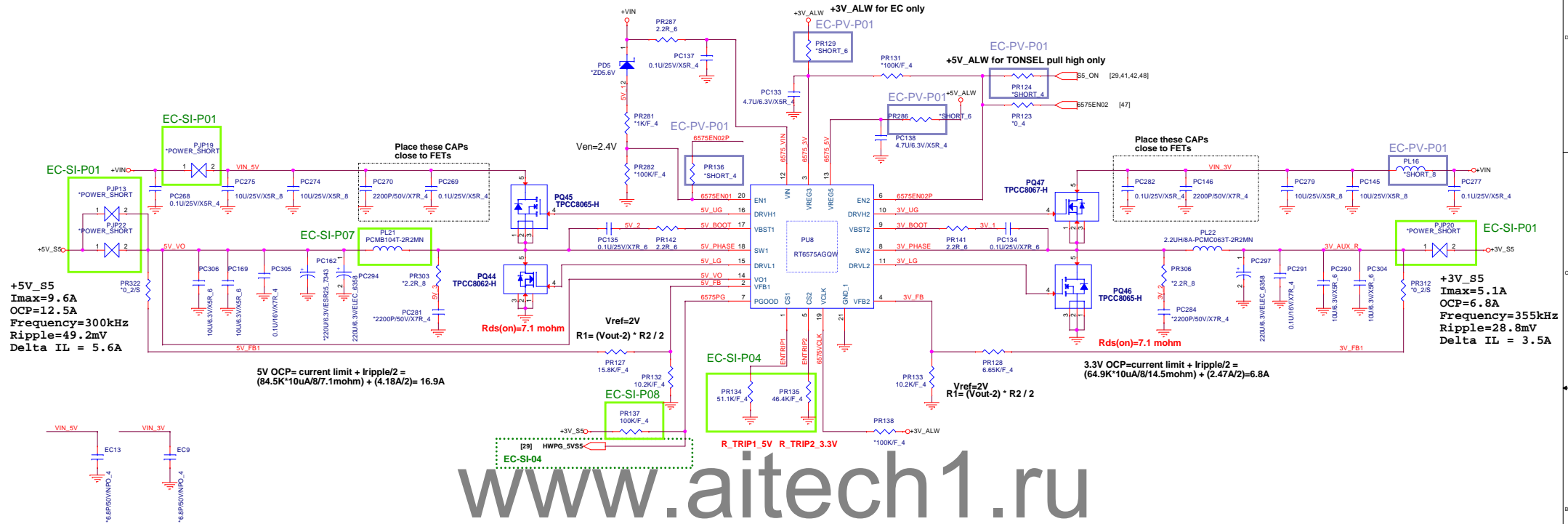






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PROJECT: HP-Hawaii



L/S Mosfet parameter

MOSFET	Package	ID (Ta=25C)	Rds_on_max
TPCC8067-H	DFN3x3	9A	26m
TPCC8062-H	DFN3x3	27A	7.1m

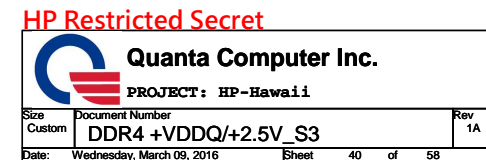
Power On sequencing

EN0	ENC	REF	VREG3	VREG5	SMPS1	SMPS2
LOW	LOW	OFF	OFF	OFF	OFF	OFF
> 2.4V	LOW	ON	ON	ON	OFF	OFF
> 2.4V	> 2.4V	ON	ON	ON	ON	ON

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Quanta Computer Inc.
PROJECT: HP-Hawaii

Size: Custom Document Number: System +3V_S5/+5V_S5 Rev: 1A
 Date: Wednesday, March 09, 2016 Sheet: 38 of 58

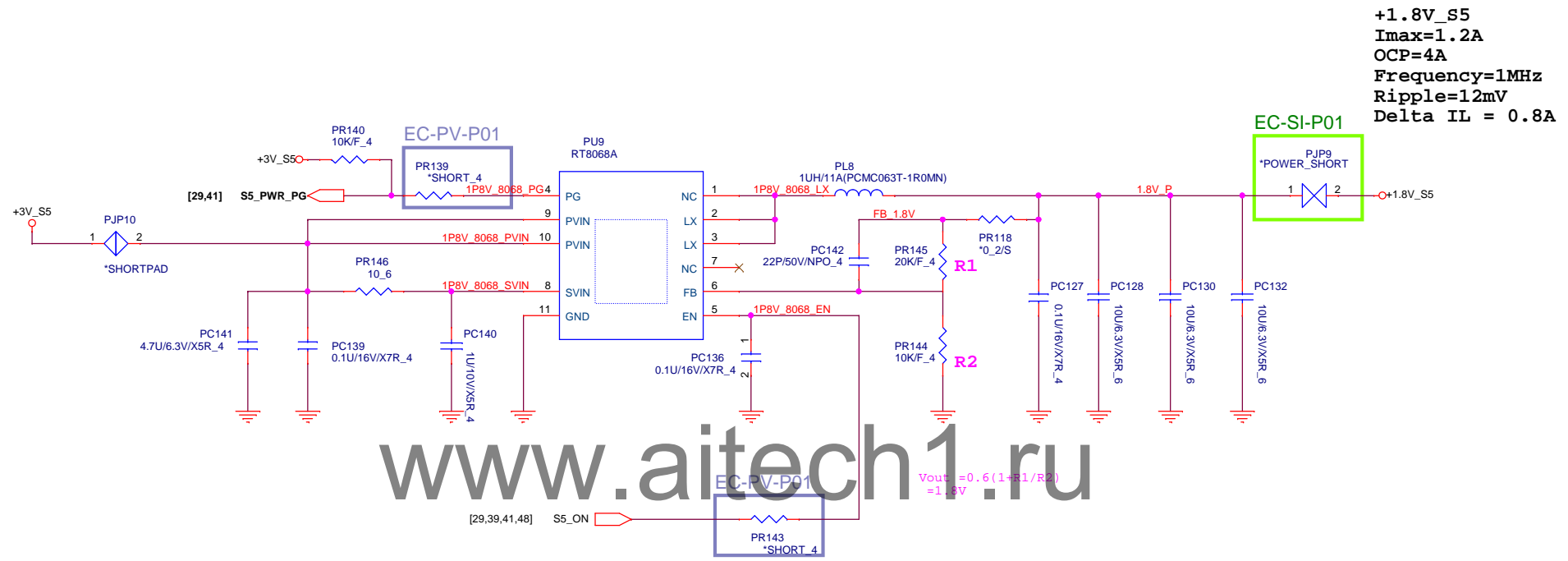


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PROJECT: HP-Hawaii

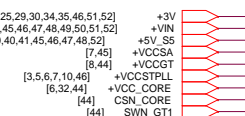
Size B	Document Number +1V_S5	Rev 1
Date:	Wednesday, March 09, 2016	Sheet 41 of 58

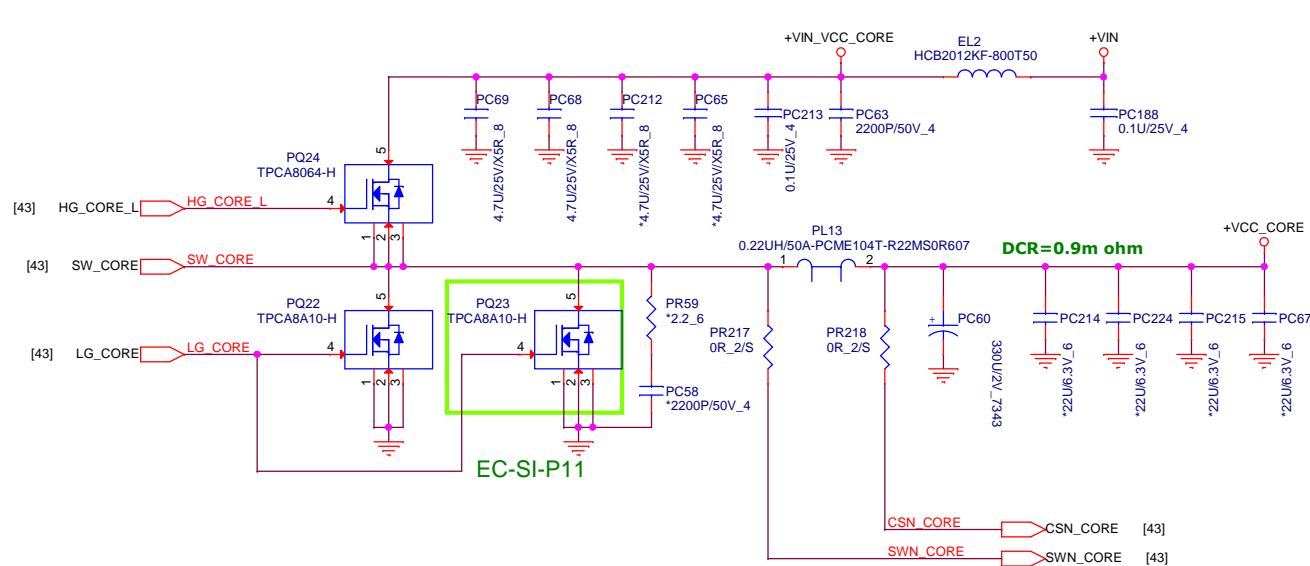


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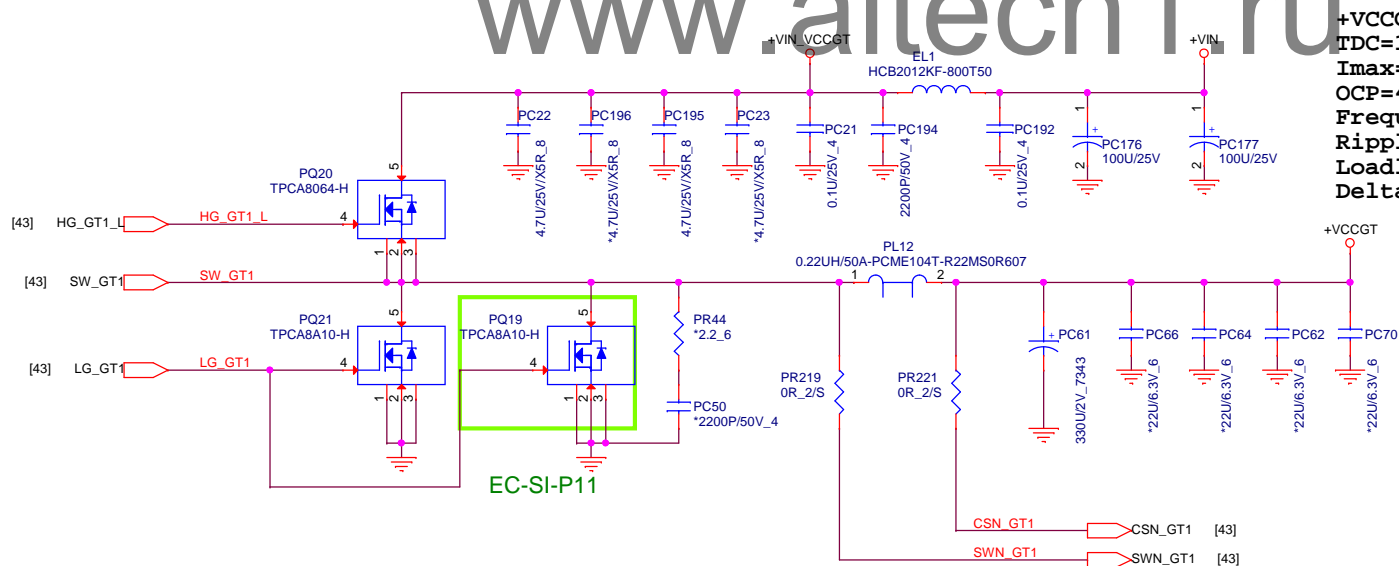
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	+1.8V_S5	
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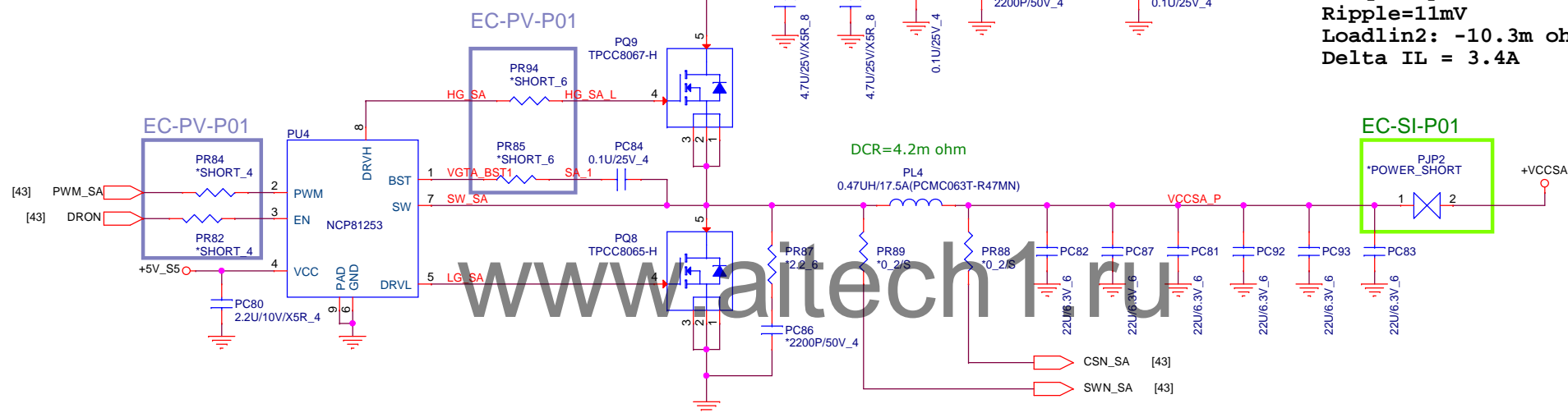
PROJECT: HP-Hawaii

Size B	Document Number	Rev 1A
	CPU +VCC_CORE/+VCCGT	
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EC-SI-P01

VCCSA
TDC=3.7A
Imax=4.5A
OCP=10A
Frequency=600KHz
Ripple=11mV
Loadlin2: -10.3m ohm
Delta IL = 3.4A

EC-SI-P01



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PROJECT: HP-Hawaii

Size
Custom

Document Number

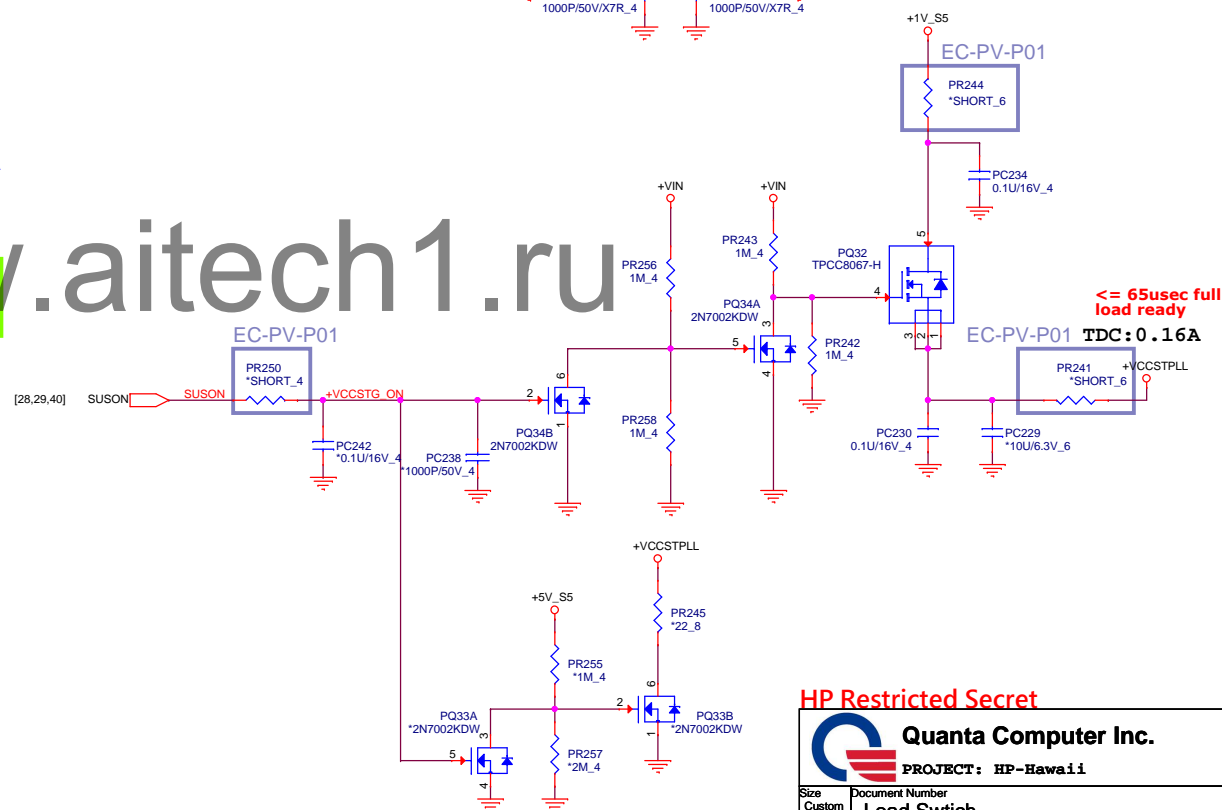
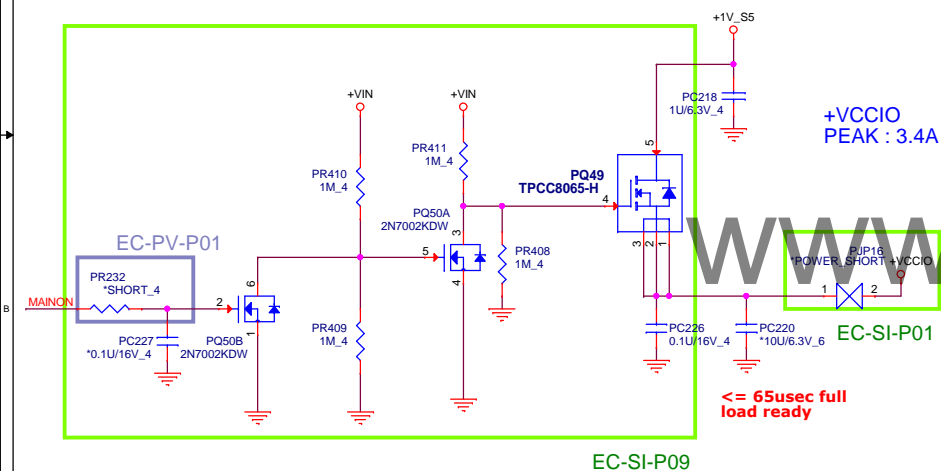
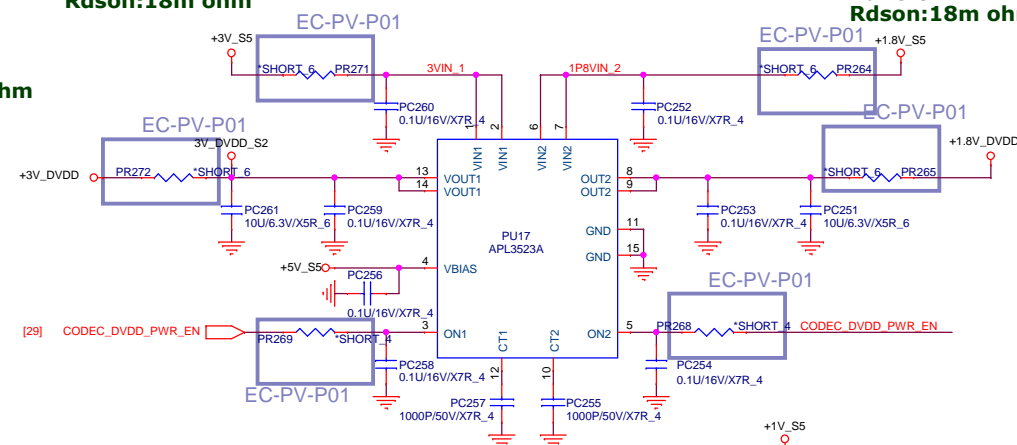
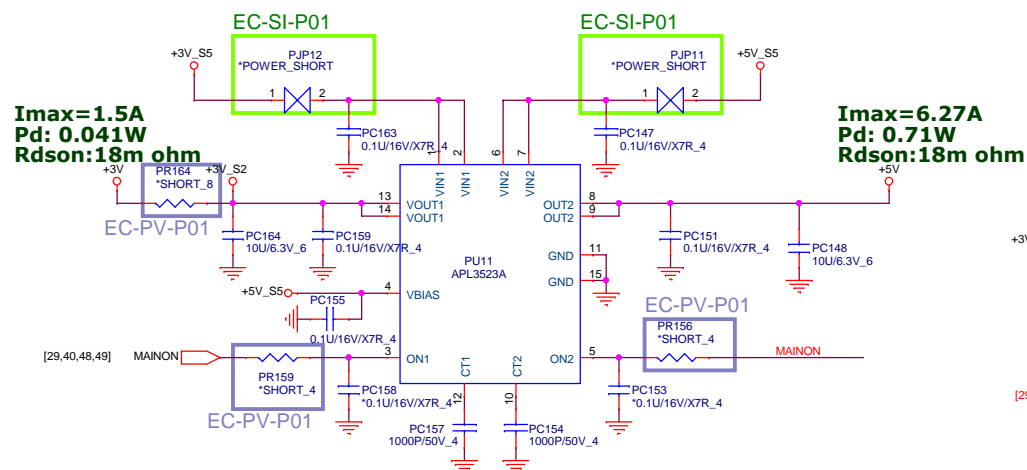
CPU + VCCSA

Rev
1/

Date: Wednesday, March 09, 2016

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0.03A
Pd: 0.01W
Rdson:18m ohm

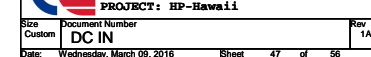


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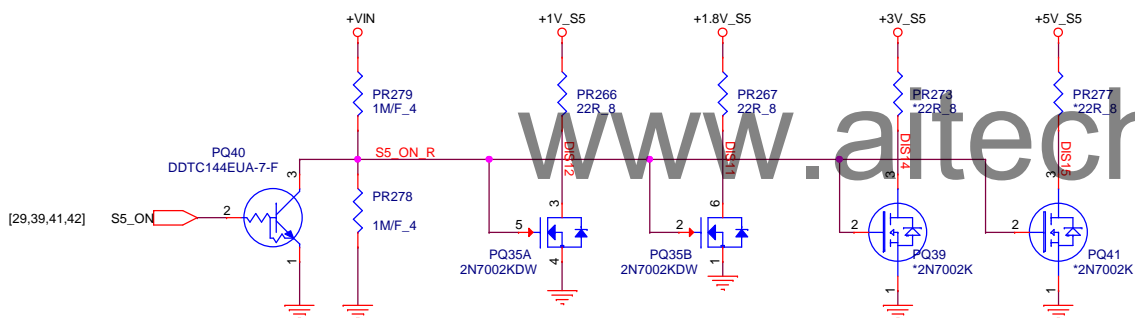
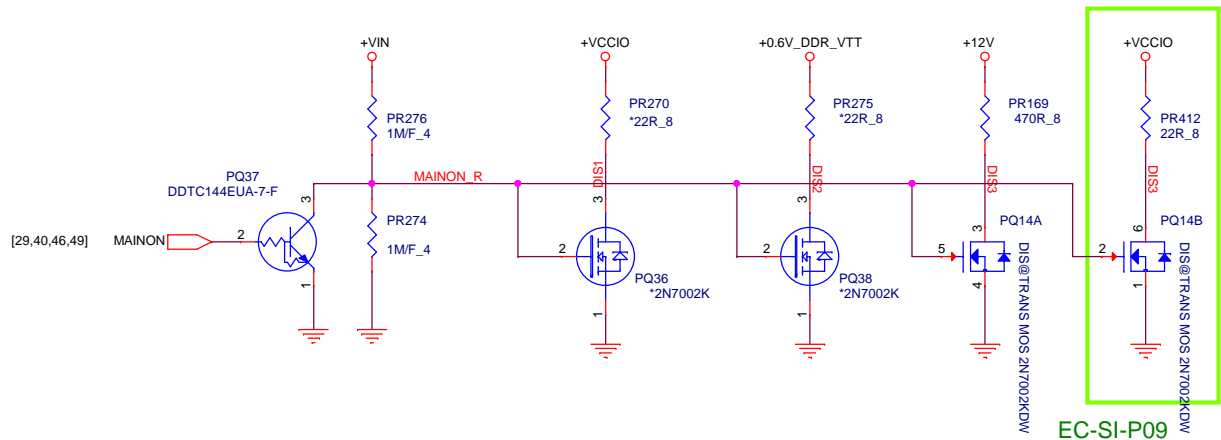
**Quanta Computer Inc.**

PROJECT: HP-Hawaii


Size Custom	Document Number Load Switch	Rev 1/
Date: Monday, March 21, 2016	Sheet 46 of 58	



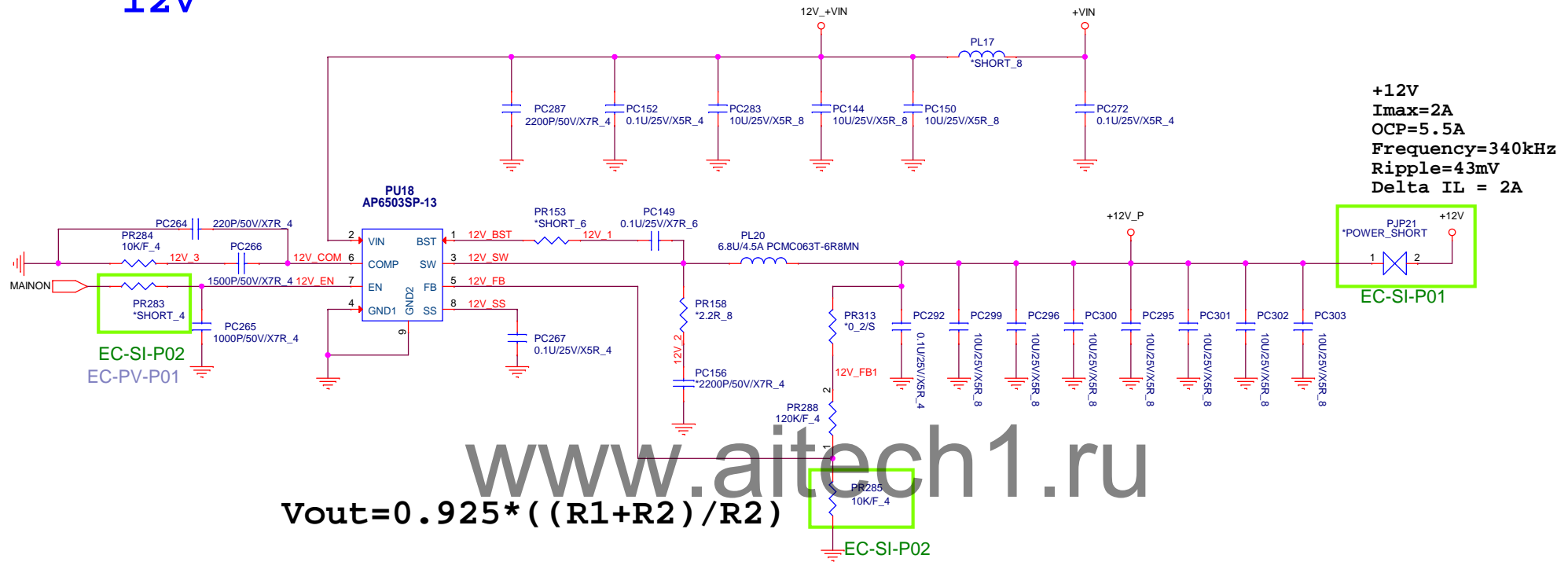
CONFIDENTIAL



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Size B	Document Number	Rev 1A
Discharge		
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12V



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PROJECT: HP-Hawaii

Size
BDocument Number
+12VRev
1A

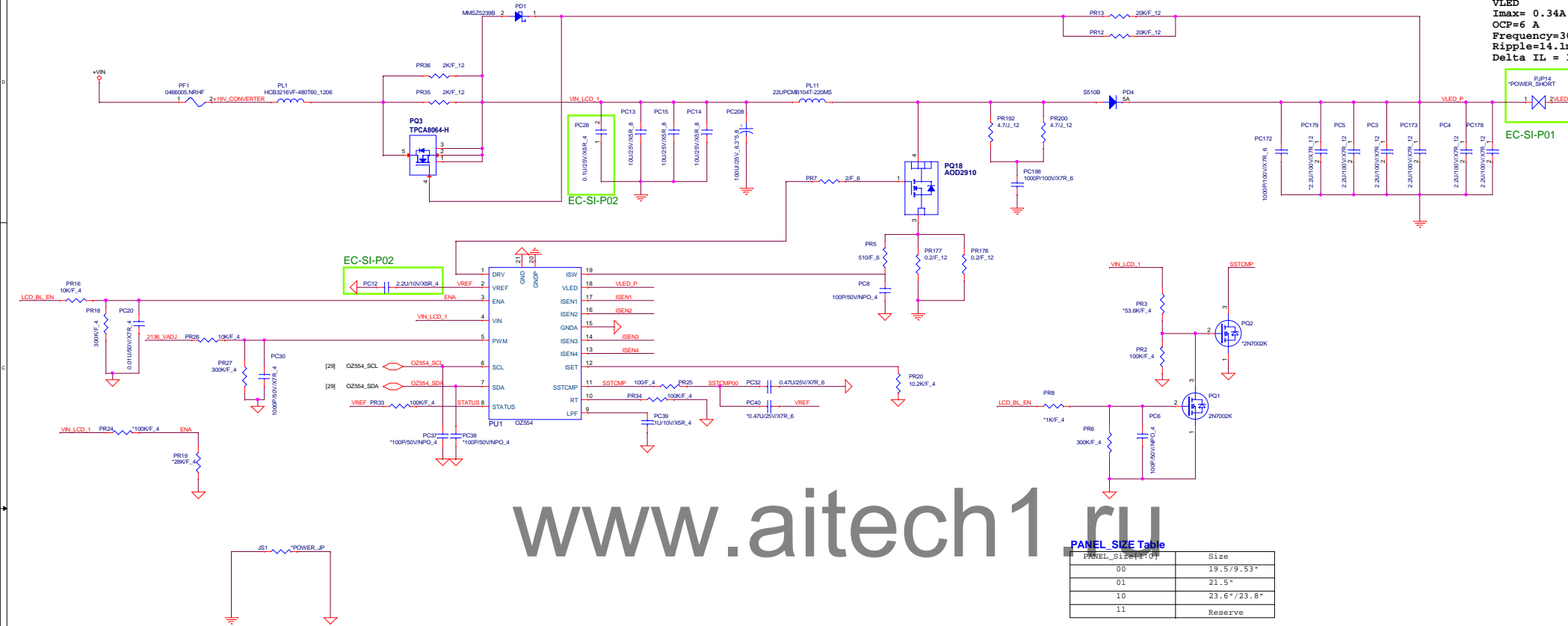
Date: Wednesday, March 09, 2016

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VLED
Imax= 0.34A
OCP=6 A
Frequency=300kHz
Ripple=14.1mV
Delta IL = 1.5 A

P1P4
POWER_SHIRT

EC-SI-P01



PANEL_SIZE Table

PANEL_Size[1:0]	Size
00	19.5"/9.53"
01	21.5"
10	23.6"/23.8"
11	Reserve

19.45" /19.53" PANEL_ID Table

PANEL_ID[3:0]	Panel model
1111	No Connect
1110	INX M200HLJ-L20 FHD
1101	AUO M195RTN01.0 HD+
1100	LGD LM195WD1-TLA1 HD+
1010	Reserve

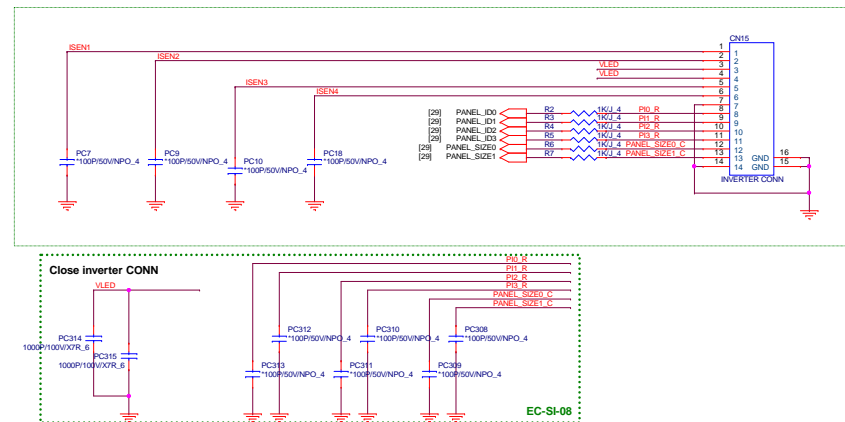
21.5" PANEL_ID Table

PANEL_ID[3:0]	Panel model
1111	No Connect
1110	INX M215HJK-L3B FHD eDP
1101	SDC LTM215HL01 FHD
1100	LGD LM215WF3-S1N1 FHD
1011	Reserve

23.6" /23.8" PANEL_ID Table

PANEL_ID[3:0]	Panel model
1111	No Connect
1110	INX M236HJK-L5B FHD eDP
1101	AUO M238HAN01.0 FHD
1100	LGD LM238WF1-S1E1 FHD
1011	SDC LTM238HL02 FHD
1010	Reserve

Panel_ID[3:0] = 1111 & Panel_Size[1:0] = 11 is reserved for cabling detection by "No connection".



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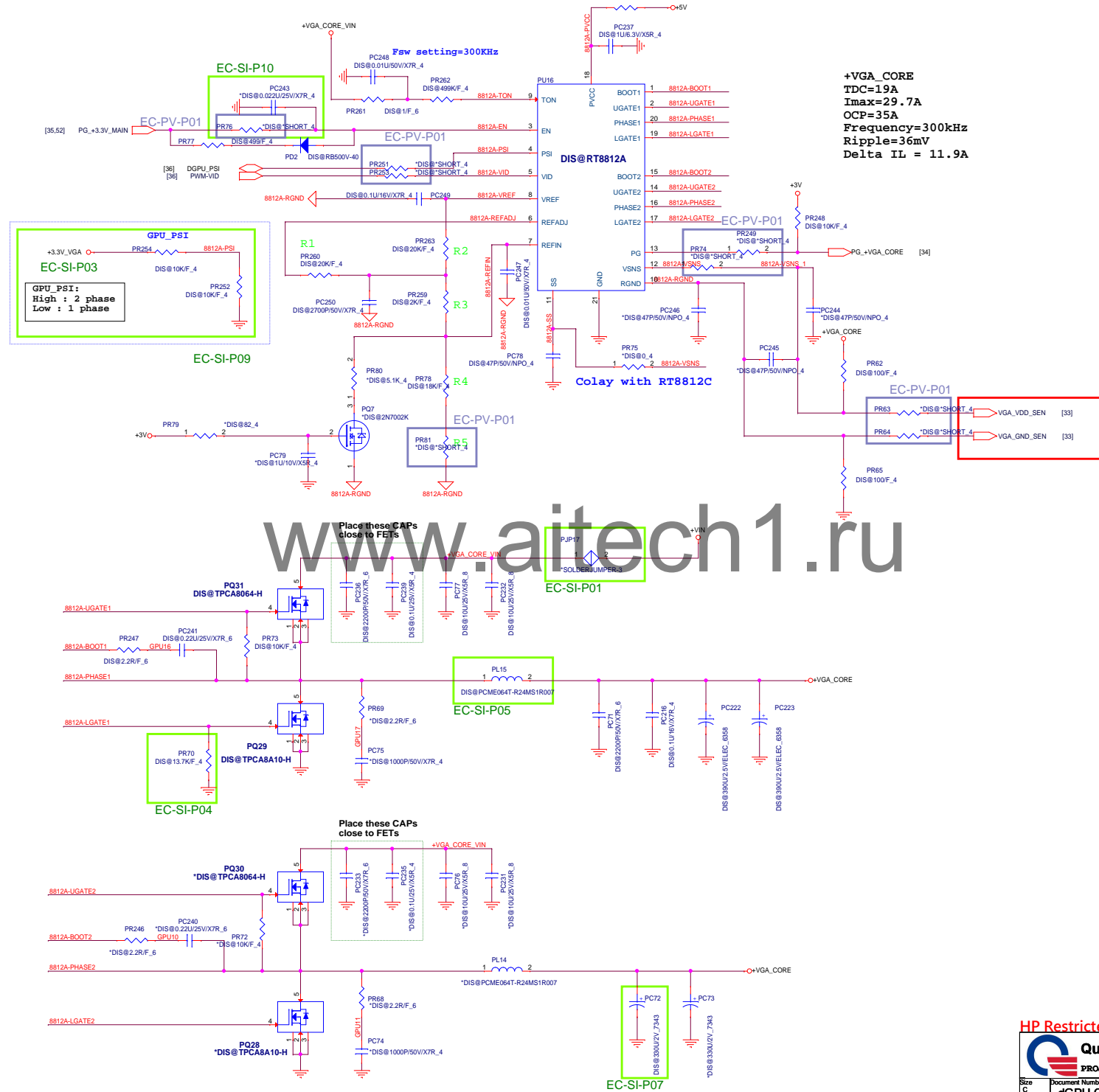
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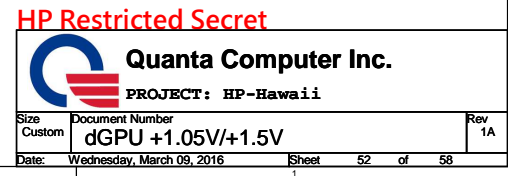


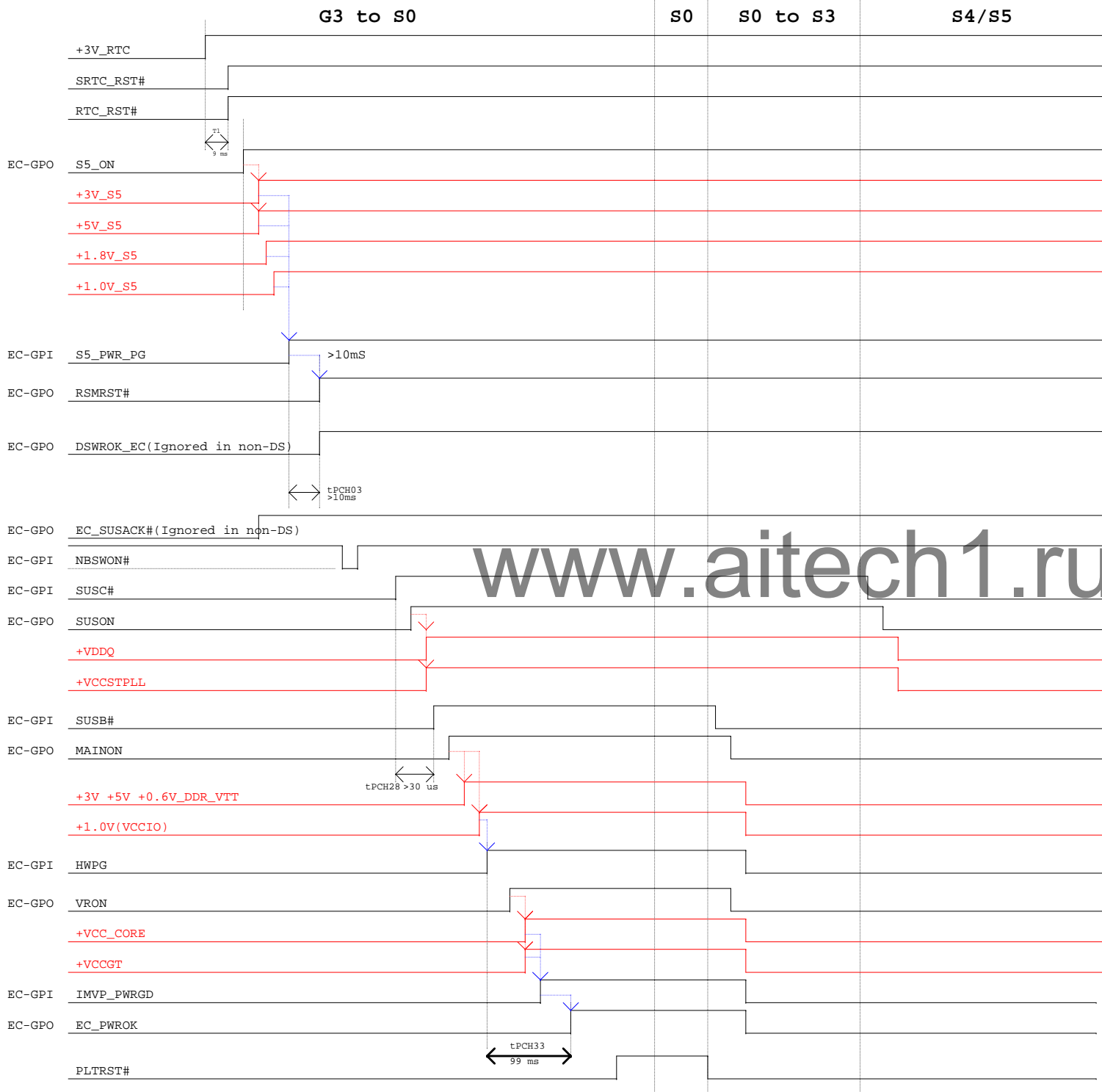
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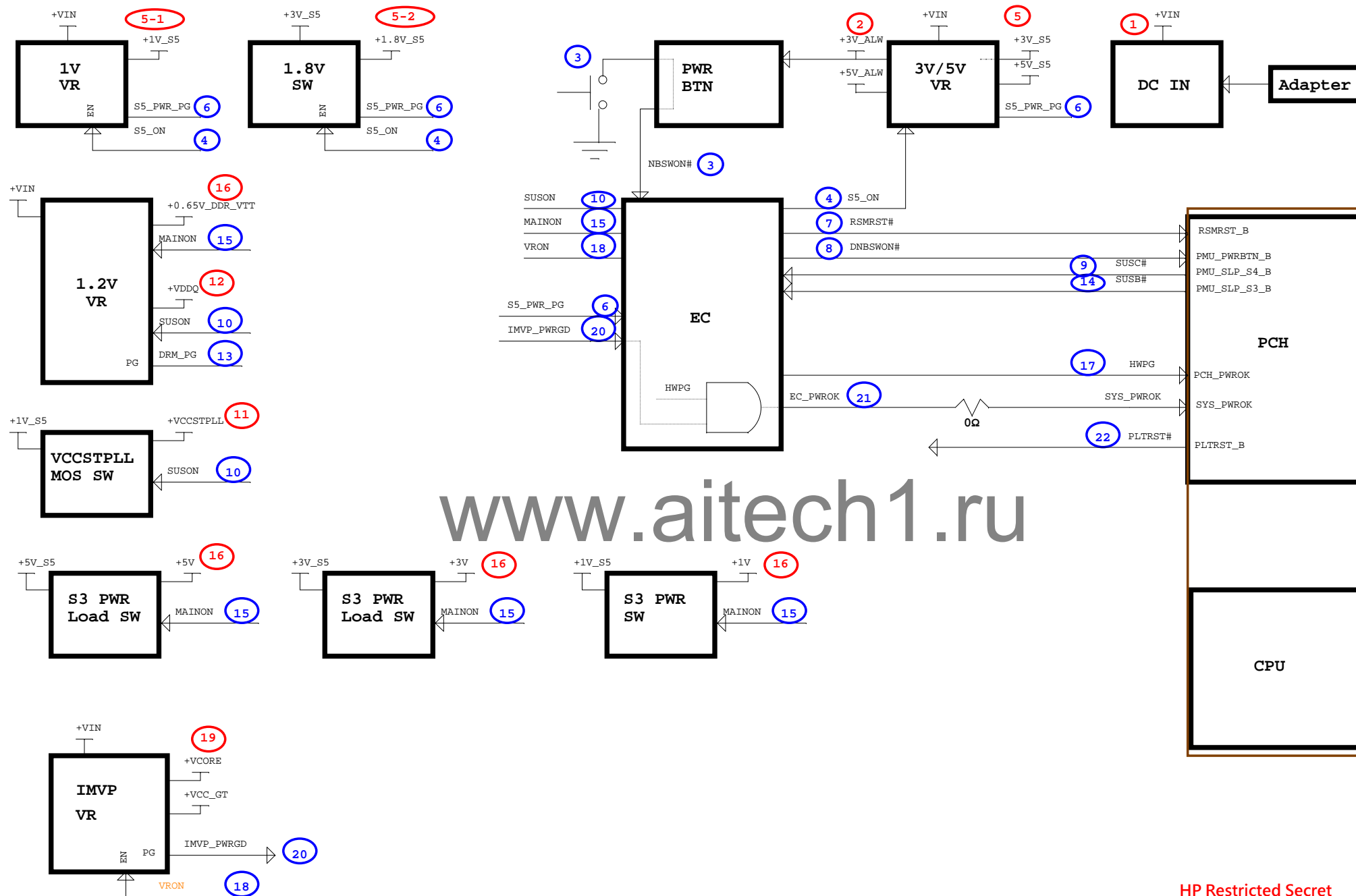


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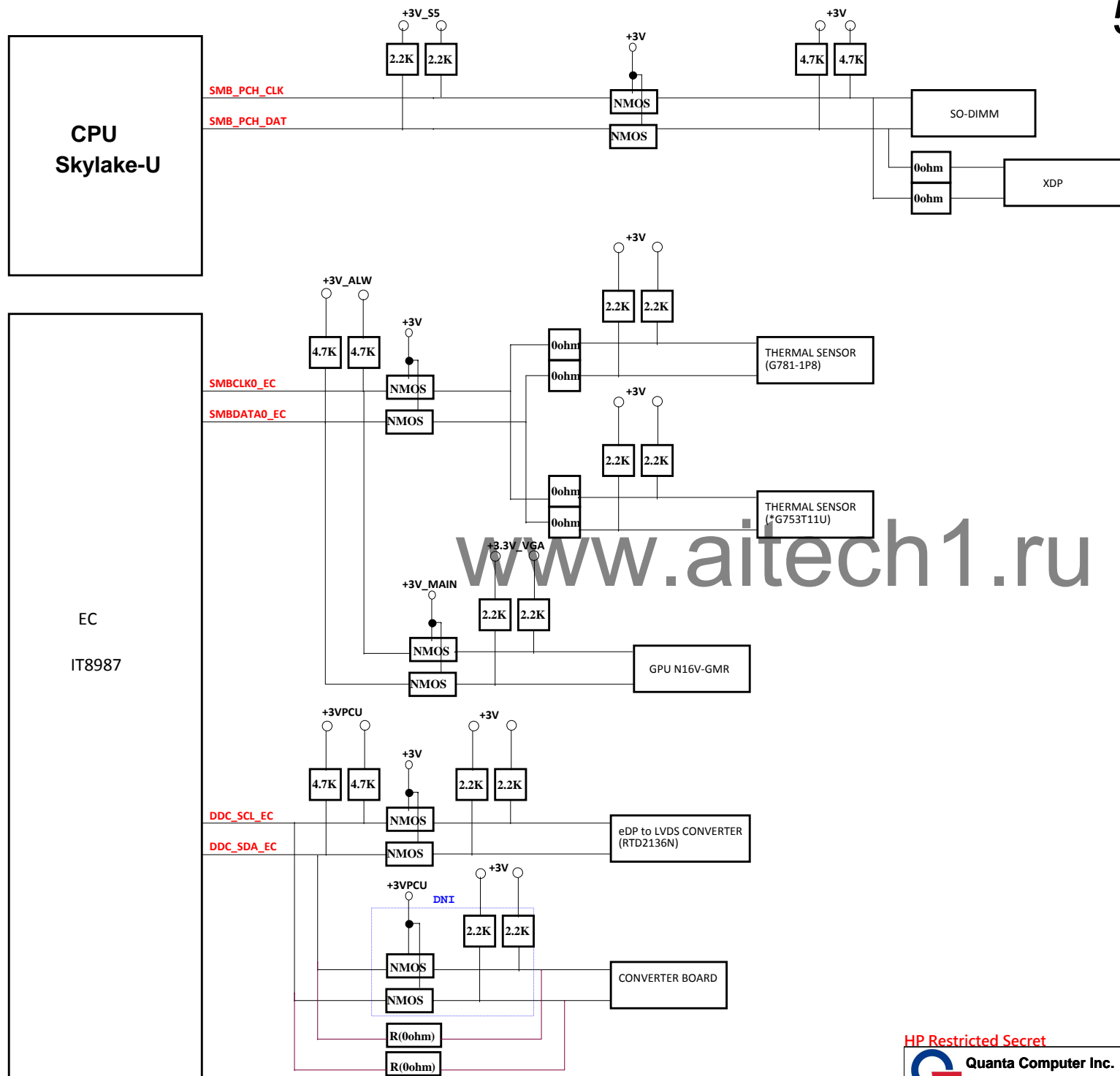


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Power sequence diagram
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N91 EE Schematic DB to SI Change List

EC#	Page	Description	Part Affected
EC-SI-01	17,18	Unstuff C205/C213 for DDR4 Issue	C205,C213
EC-SI-02	21	Change HDMI HPD signal from low active to high active	Q38,R638,R639
EC-SI-03	21	Modify Q37 MOSFET gate power source from +5V to +3V	Q37
EC-SI-04	28	Swap EC GPIO for reserving 2nd fan control	
EC-SI-05	22	Separate L/R channels for speaker connector	CN26,CN27
EC-SI-06	20	Add ESD protection for CCD	
EC-SI-07	29	Reserve 2nd FAN	
EC-SI-08	49	Reserve 100pF for CN15 (EMI suggestion)	
EC-SI-09	31	Add 2 GND pad for EMI	
EC-SI-10	25	Change ODD connector	CN21
EC-SI-11	26	Change connector of card reader daughter board	CN24
EC-SI-12	13,34	Change load cap for 32.768K/24M/27M due to vendor suggest	
EC-SI-13	All	Stuff EMC/ESD/RF materials	
EC-SI-14	35	Unstuff R437 for correct PSI setting	R437
EC-SI-15	22	Change AL7/AL8/AL9/AL11 as 0ohm from Realtek suggest	AL7,AL8,AL9,AL11

N91 EE Schematic SI to PV Change List

EC#	Page	Description	Part Affected
EC-PV-01	All	Change 0ohm resistor to be short pad	
EC-PV-02	27	Remove reserved CMC of USB3.0	L28,L29,L30,L33

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N91 Power Schematic DB to SI Change List

EC#	Page	Description	Part Affected
EC-SI-P01	38~51	Change default open to default short	PJP1~PJP22
EC-SI-P02	48,49,51	Downsize components	PR283, PR285, PC12, PC28, PC184, PC185, PC174, PL3
EC-SI-P03	50, 51	Correct connection	
EC-SI-P04	38,40,42,50	Fine tune OCP function	PR134, PR135, PR101, PR21, PR70
EC-SI-P05	50	Change choke for transient	PL15
EC-SI-P06	40,51	Fine tune offset voltage	PR97, PR186
EC-SI-P07	38, 50	Change components for ripple voltage	PL21, PC72
EC-SI-P08	38,39	Add components for PG function	PR137, PR122
EC-SI-P09	39,40,45~47,50,51	Change components for common part using	PU6, PQ10, PQ13, PQ14, PQ49, PQ50, PR408~PR412, PR254, PR252, PQ4, PQ5, PQ26, PR172
EC-SI-P10	50	Fine tune soft start	PR76, PC243
EC-SI-P11	43	Add components for Efficiency	PQ19, PQ23
EC-SI-P12	42	Fine tune DVID setting	PR210, PR22
EC-SI-P13	42	Fine tune lout function	PR205, PR209, PC54, PC204
EC-SI-P14	42	Fine tune compensation	PR31, PC205

N91 EE Schematic SI to PV Change List

EC#	Page	Description	Part Affected
EC-PV-P01	All	Change 0ohm resistor to short pad	
EC-PV-P02	42	Fine tune +VCCGT load line	PR14
EC-PV-P03	42	Fine tune +VCCGT lout function	PR195
EC-PV-P04	42	Fine tune Vcore OCP	PR208
EC-PV-P05	42	Fine tune Vcore lout function	PR209
EC-PV-P06	42	Fine tune Vcore Loadline	PR212, PR214

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